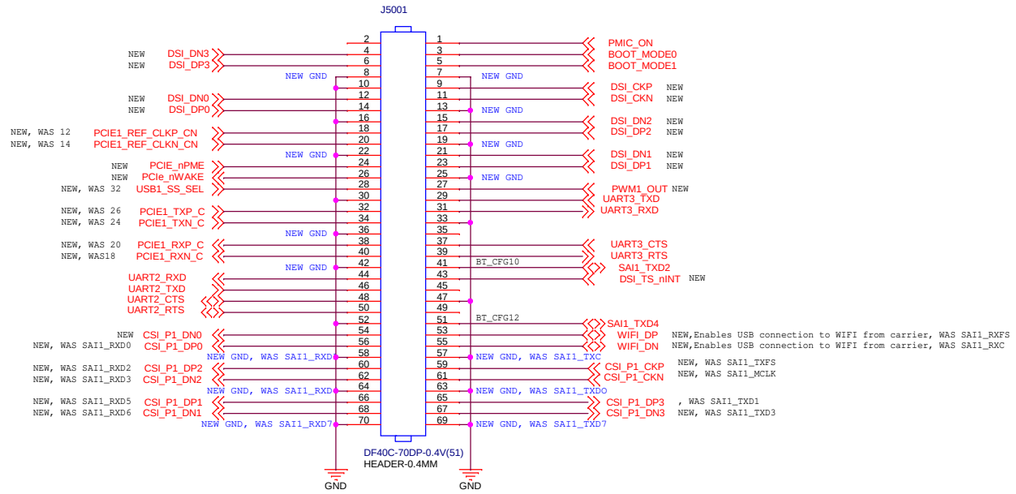
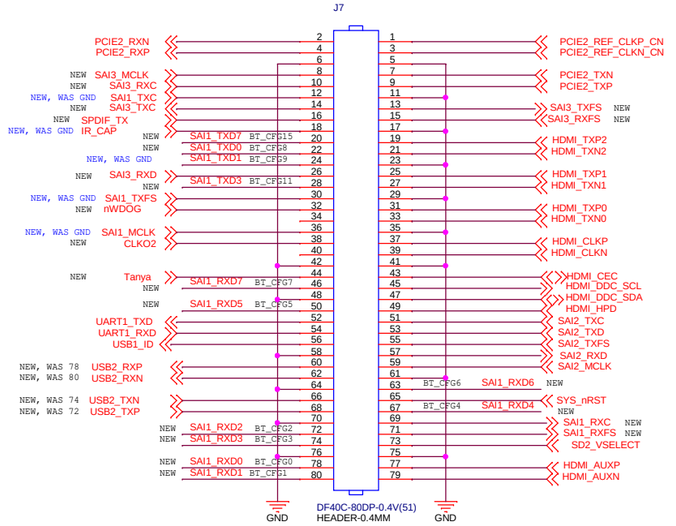
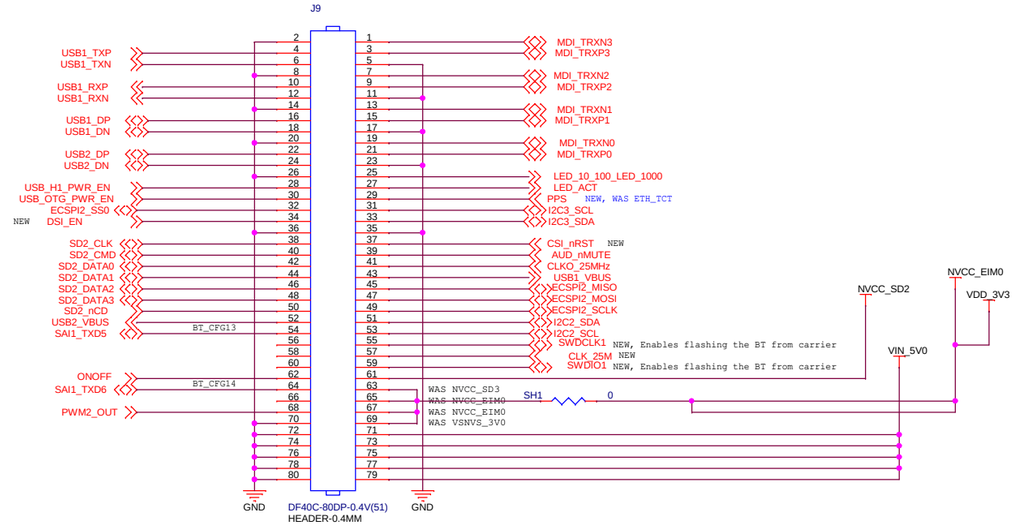
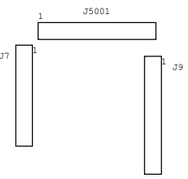
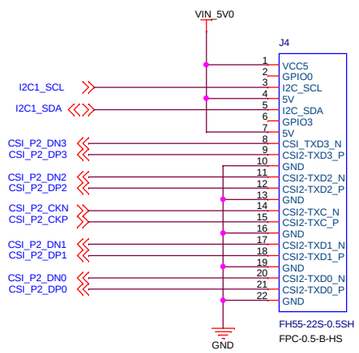






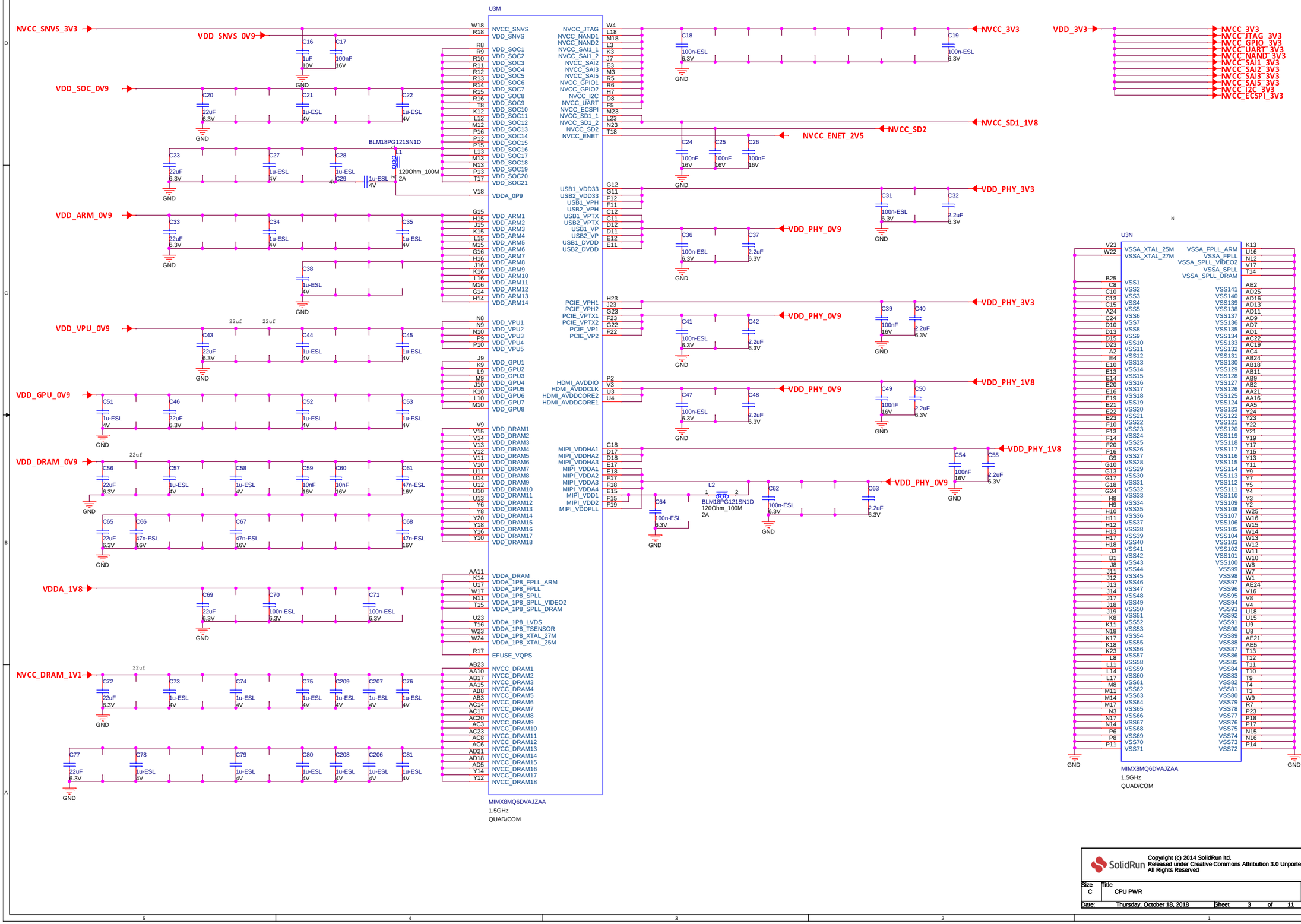




Size	Title	Rev
C	B-T-B CONNECTORS	1.0

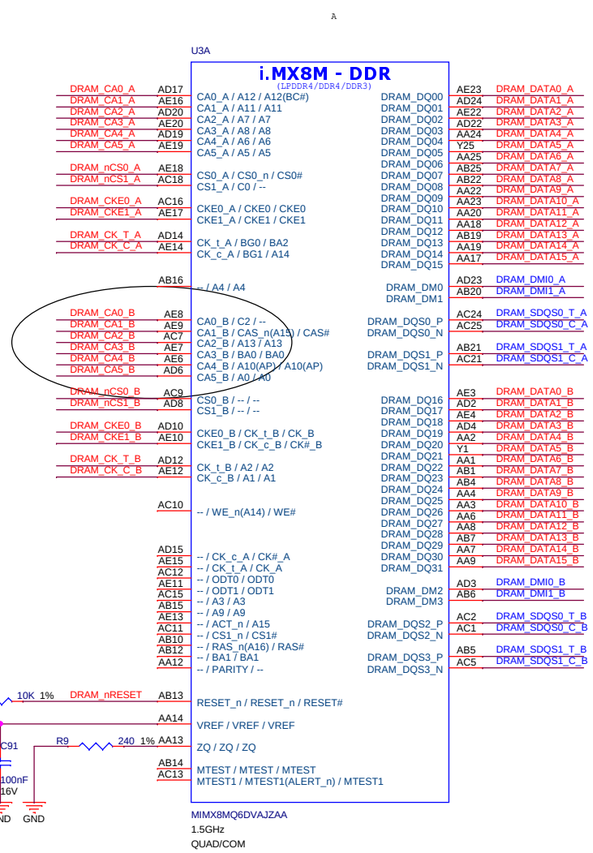
Date: Thursday, October 18, 2018 Sheet 1 of 11

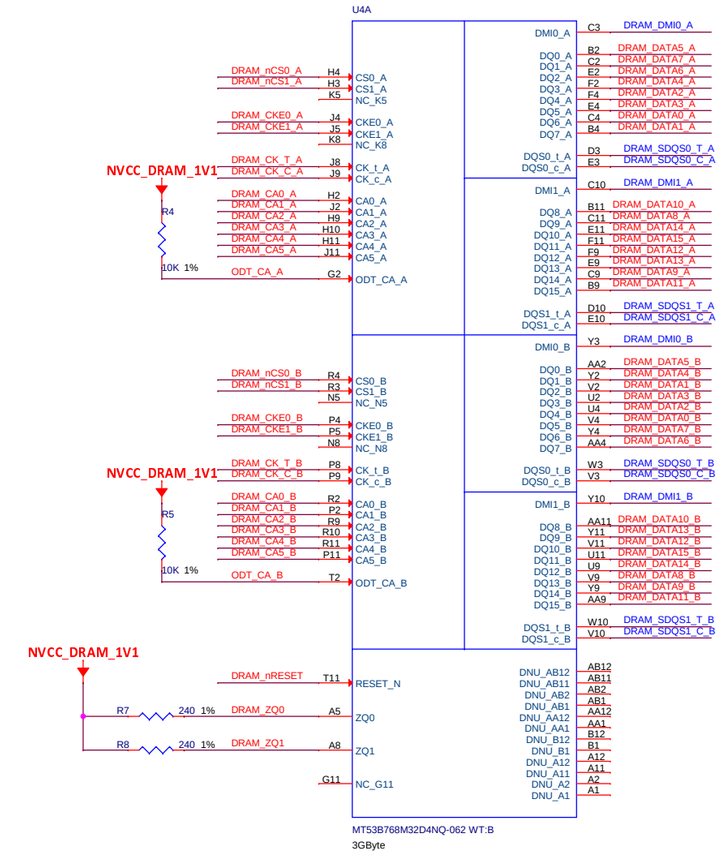
mScale850 PWR

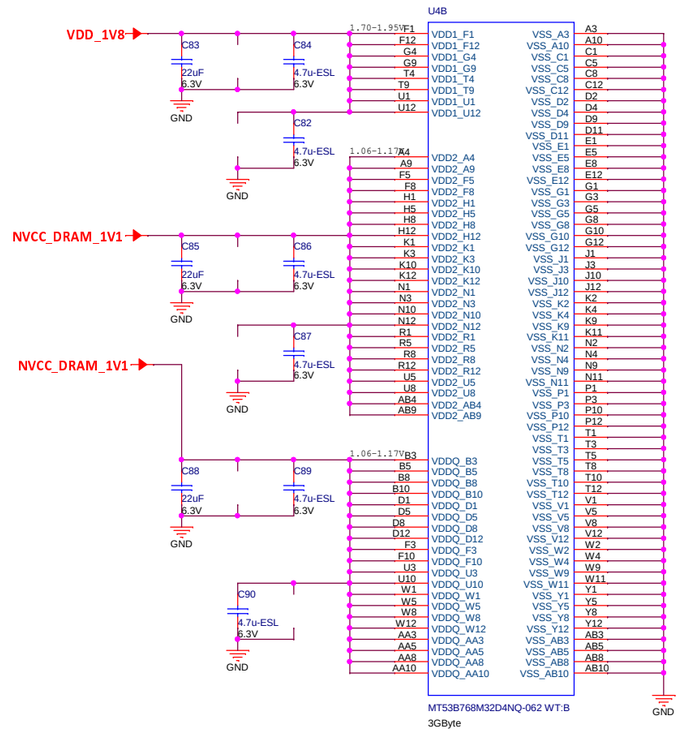


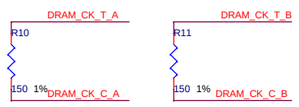
Size	Title	Rev
C	CPU PWR	1.0
Date: Thursday, October 18, 2018	Sheet 3 of 11	

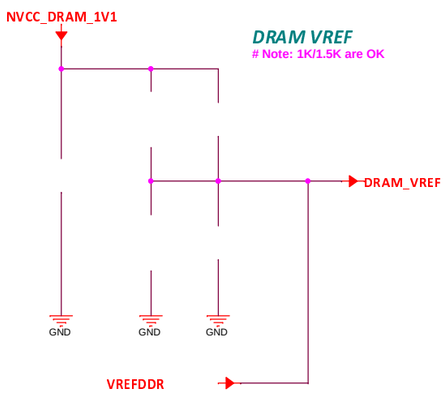
LPDDR4











Size	Title	Rev
C	LPDDR4	1.0

Date: Saturday, December 08, 2018 Sheet 4 of 11

-Internal pullup resistors 27 kOhm;
-Internal pulldown resistor of 90kOhm is always enabled

U3H

i.MX8M - NAND

NVCC_NAND

NAND_CE0_B	H19	NAND_nCE0	QSPIA_nSS0
NAND_CE1_B	G21	NAND_nCE1	USB_OTG_PWR_EN
NAND_CE2_B	F21	NAND_nCE2	REF_CLK_32K
NAND_CE3_B	H20		USB_H1_PWR_EN
NAND_ALE	G19	NAND_ALE	QSPIA_SCLK
NAND_CLE	H21	NAND_CLE	PCIE_nPME
NAND_RE_B	K19	NAND_nRE	USB1_SS_SEL
NAND_WE_B	K22		
NAND_WP_B	K21		
NAND_READY_B	K20		
NAND_DQS	M20		
NAND_DATA00	G20	NAND_DATA0	QSPIA_DATA0
NAND_DATA01	J20	NAND_DATA1	QSPIA_DATA1
NAND_DATA02	H22	NAND_DATA2	QSPIA_DATA2
NAND_DATA03	J21	NAND_DATA3	QSPIA_DATA3
NAND_DATA04	L20		
NAND_DATA05	J22		CLKO_25MHz
NAND_DATA06	L19		PCIe_nWAKE
NAND_DATA07	M19		

MIMX8MQ6DVAJZAA
1.5GHz
QUAD/COM

U3J

i.MX8M - eNET

NVCC_ENET

ENET_MDC	N20	ENET_MDC	ENET_MDC
ENET_MDIO	N19	ENET_MDIO	ENET_MDIO
ENET_TX_CTL	P19	ENET_TX_CTL	ENET_TX_CTL
ENET_TXC	T19	ENET_TXC	ENET_TXC
ENET_TD0	R20	ENET_TD0	ENET_TD0
ENET_TD1	R21	ENET_TD1	ENET_TD1
ENET_TD2	R19	ENET_TD2	ENET_TD2
ENET_TD3	P20	ENET_TD3	ENET_TD3
ENET_RX_CTL	T21	ENET_RX_CTL	ENET_RX_CTL
ENET_RXC	T20	ENET_RXC	ENET_RXC
ENET_RD0	U19	ENET_RD0	ENET_RD0
ENET_RD1	U21	ENET_RD1	ENET_RD1
ENET_RD2	U20	ENET_RD2	ENET_RD2
ENET_RD3	V19	ENET_RD3	ENET_RD3

MIMX8MQ6DVAJZAA
1.5GHz
QUAD/COM

U3I

i.MX8M - SD

NVCC_SD1

SD1_CLK	R43	0	L25 SD1_CLK
SD1_CMD			L24 SD1_CMD
SD1_DATA0			M25 SD1_DATA0
SD1_DATA1			M24 SD1_DATA1
SD1_DATA2			N25 SD1_DATA2
SD1_DATA3			P25 SD1_DATA3
SD1_DATA4			N24 SD1_DATA4
SD1_DATA5			P24 SD1_DATA5
SD1_DATA6			R25 SD1_DATA6
SD1_DATA7			T25 SD1_DATA7
SD1_nRST			R24 SD1_RESET_B
SD1_STROBE			T24 SD1_STROBE

NVCC_SD2

SD2_CLK	L22	SD2_CLK	SD2_CLK
SD2_CMD	M22	SD2_CMD	SD2_CMD
SD2_DATA0	N22	SD2_DATA0	SD2_DATA0
SD2_DATA1	N21	SD2_DATA1	SD2_DATA1
SD2_DATA2	P22	SD2_DATA2	SD2_DATA2
SD2_DATA3	P21	SD2_DATA3	SD2_DATA3
SD2_WP	M21		
SD2_CD_B	L21	SD2_nCD	SD2_nCD
SD2_RESET_B	R22		

MIMX8MQ6DVAJZAA
1.5GHz
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U3G

i.MX8M - SAI

NVCC_SAI3

SAI5_MCLK	K4		
SAI5_RXFS	N4		
SAI5_RXC	L5		
SAI5_RXD0	M5		
SAI5_RXD1	L4		
SAI5_RXD2	M4		
SAI5_RXD3	K5		
SAI3_MCLK	D3	SAI3_MCLK	SAI3_MCLK
SAI3_TXFS	G3	SAI3_TXFS	SAI3_TXFS
SAI3_TXC	C4	SAI3_TXC	SAI3_TXC
	C3		UBLOX_RSTN
SAI3_RXFS	G4	SAI3_RXFS	SAI3_RXFS
SAI3_RXC	F4	SAI3_RXC	SAI3_RXC
SAI3_RXD	F3	SAI3_RXD	SAI3_RXD
SPDIF_TX	F6	SPDIF_TX	SPDIF_TX
SPDIF_RX	G6		
SPDIF_EXT_CLK	E6		WL_REG_ON

NVCC_SAI1

SAI1_MCLK	A3	SAI1_MCLK	SAI1_MCLK
SAI1_TXFS	H1	SAI1_TXFS	SAI1_TXFS
SAI1_TXC	E1	SAI1_TXC	SAI1_TXC
SAI1_TXD0	F2	SAI1_TXD0	SAI1_TXD0
SAI1_TXD1	E2	SAI1_TXD1	SAI1_TXD1
SAI1_TXD2	B2	SAI1_TXD2	SAI1_TXD2
SAI1_TXD3	D1	SAI1_TXD3	SAI1_TXD3
SAI1_TXD4	D2	SAI1_TXD4	SAI1_TXD4
SAI1_TXD5	C2	SAI1_TXD5	SAI1_TXD5
SAI1_TXD6	B3	SAI1_TXD6	SAI1_TXD6
SAI1_TXD7	C1	SAI1_TXD7	SAI1_TXD7
SAI1_RXFS	L1	SAI1_RXFS	SAI1_RXFS
SAI1_RXC	K1	SAI1_RXC	SAI1_RXC
SAI1_RXD0	K2	SAI1_RXD0	SAI1_RXD0
SAI1_RXD1	L2	SAI1_RXD1	SAI1_RXD1
SAI1_RXD2	H2	SAI1_RXD2	SAI1_RXD2
SAI1_RXD3	J2	SAI1_RXD3	SAI1_RXD3
SAI1_RXD4	J1	SAI1_RXD4	SAI1_RXD4
SAI1_RXD5	F1	SAI1_RXD5	SAI1_RXD5
SAI1_RXD6	G2	SAI1_RXD6	SAI1_RXD6
SAI1_RXD7	G1	SAI1_RXD7	SAI1_RXD7

NVCC_SAI2

SAI2_MCLK	H5	SAI2_MCLK	SAI2_MCLK
SAI2_TXFS	H4	SAI2_TXFS	SAI2_TXFS
SAI2_TXC	J5	SAI2_TXC	SAI2_TXC
SAI2_TXD0	G5	SAI2_TXD	SAI2_TXD
	J4		WL_nPERST
SAI2_RXFS	H3		
SAI2_RXC	H6	SAI2_RXD	SAI2_RXD
SAI2_RXD0			

MIMX8MQ6DVAJZAA
1.5GHz
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U3K

NVCC_ECSPI1

ECSPI1_SS0	D4	ECSPI1_SS0	UART3_RTS
ECSPI1_MOSI	A4	ECSPI1_MOSI	DSI_TS_nINT
ECSPI1_MISO	B4	ECSPI1_MISO	UART3_CTS
ECSPI1_SCLK	D5	ECSPI1_SCLK	DSI_EN

NVCC_ECSPI2

ECSPI2_SS0	A5	ECSPI2_SS0	ECSPI2_SS0
ECSPI2_MOSI	E5	ECSPI2_MOSI	ECSPI2_MOSI
ECSPI2_MISO	B5	ECSPI2_MISO	ECSPI2_MISO
ECSPI2_SCLK	C5	ECSPI2_SCLK	ECSPI2_SCLK

NVCC_GPIO1

GPIO1_IO00	T6		
GPIO1_IO01	T7	GPIO1_IO01	PWM1_OUT
GPIO1_IO02	R4	GPIO1_IO02	nWDOG
GPIO1_IO03	P4		
GPIO1_IO04	P5	GPIO1_IO04	SD2_VSELECT
GPIO1_IO05	P7		
GPIO1_IO06	N5	GPIO1_IO06	CSI_nRST
GPIO1_IO07	N6	GPIO1_IO07	PMIC_nINT
GPIO1_IO08	N7	GPIO1_IO08	AUD_nMUTE
GPIO1_IO09	M6	GPIO1_IO09	ENET_nRST
GPIO1_IO10	M7	GPIO1_IO10	ENET_WoL
GPIO1_IO11	L6	GPIO1_IO11	ENET_nINT
GPIO1_IO12	L7	GPIO1_IO12	IR_CAP
GPIO1_IO13	K6	GPIO1_IO13	PWM2_OUT
GPIO1_IO14	K7		
GPIO1_IO15	J6	GPIO1_IO15	CLKO2

NVCC_I2C

UART1_RXD	C7	UART1_RXD	J7, DEBUG MCU
UART1_TXD	A7	UART1_TXD	J7, DEBUG MCU
UART2_RXD	B6	UART2_RXD	J5001 DEBUG CPU
UART2_TXD	D6	UART2_TXD	J5001 DEBUG CPU
UART3_RXD	A6	UART3_RXD	J5001
UART3_TXD	B7	UART3_TXD	J5001
UART4_RXD	C6	UART2_CTS	J5001 WAS WL_nPERST
UART4_TXD	D7	UART2_RTS	J5001 WAS WL_REG_ON
I2C1_SCL	E7	I2C1_SCL	SOM, PMIC Was USB
I2C1_SDA	E8	I2C1_SDA	SOM, PMIC Was USB
I2C2_SCL	G7	I2C2_SCL	J9
I2C2_SDA	F7	I2C2_SDA	J9
I2C3_SCL	G8	I2C3_SCL	J9
I2C3_SDA	E9	I2C3_SDA	J9
I2C4_SCL	F8	PCIE1_nCLKREQ	WIFI MODULE
I2C4_SDA	F9	Tanya	

MIMX8MQ6DVAJZAA
1.5GHz
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NVCC_I2C_3V3

R14	4.7K	5%	I2C1_SCL
R15	4.7K	5%	I2C1_SDA
R16	4.7K	5%	I2C2_SCL
R17	4.7K	5%	I2C2_SDA
R18	4.7K	5%	I2C3_SCL
R19	4.7K	5%	I2C3_SDA

Size	Title	Rev
C	CPU IO	1.0
Date: Thursday, October 18, 2018	Sheet 5 of 11	

BOOT_MODE0
BOOT_MODE1
ONOFF
PMIC_STBY_REQ
PMIC_ON_REQ

JTAG Debug

POR_B
R20 1K 5%
C92 100nF 16V
GND

NVCC_SNVS_3V3
R22 4.7K 5%
J5001 ONOFF
PMIC_STBY_REQ
PMIC_ON_REQ

U3L
i.MX8M - MISC
ONOFF
POR_B
PMIC_STBY_REQ
PMIC_ON_REQ
RTC
RTC_RESET_B
BOOT_MODE0
BOOT_MODE1
TEST_MODE
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST_B
JTAG_MOD
NVCC_SNVS
NVCC_JTAG
XTALI_25M
XTALO_25M
XTALI_27M
XTALO_27M
VDDA
CLK1_P
CLK1_N
CLK2_P
CLK2_N
MIMX8MQ6DVAJZAA
1.5GHz
QUAD/COM

TP4 JTAG_nTRST
TP5 JTAG_TDI
TP6 JTAG_TMS
TP7 JTAG_TCK
TP8 JTAG_TDO
TP9 POR_B
R21 10K 1%

W21 ONOFF
W20 POR_B
V21 PMIC_STBY_REQ
V20 PMIC_ON_REQ
V22 RTC_CLK_32K768
W19 RTC_RESET_B
U25 XTALI_25M
U24 XTALO_25M
V25 XTALI_27M
V24 XTALO_27M
W6 BOOT_MODE0
V6 BOOT_MODE1
V7 TEST_MODE
T5 JTAG_TCK
V5 JTAG_TMS
W5 JTAG_TDI
U5 JTAG_TDO
U6 JTAG_nTRST
U7 JTAG_MOD
R23 0
R24 10K 1%
R23 T23 Check B-t-B input
T22 CLK2_P WI-FI MODULE
U22 CLK2_N WI-FI MODULE output
R25 100 1%

NVCC_SNVS_3V3
OSC1
VCC OUT
VIO GND
32.768KHZ
C93 100nF 16V
GND

NVCC_SNVS_3V3
R26 1.5K 1%
C94 100nF 16V
U5 2.6V
VIN RST
GND NC
NCP305LSQ26T1G

Y1 25.00MHz 2.0x1.6
18pF/10PPM
C95 18pF 50V
C96 18pF 50V

Y2 27 MHz 2.0x1.6
10pF/10PPM
C97 18pF 50V
C98 18pF 50V

Size	Title	Rev
C	CPU PERI2	1.0
Date: Wednesday, October 24, 2018	Sheet 6 of 11	

mScale850 PHY

VDD_PHY_3V3 → VDD_PHY_3V3
VDD_PHY_1V8 → VDD_PHY_1V8
VDD_PHY_0V9 → VDD_PHY_0V9

USB_RESREF: Attach a 200-¦, 1% 100-ppm/C precision resistor-to-ground on the board.
MIPIDSI_REXT: 15K-¦.
PCIE: 200-¦.¡Â¼% ¡Â 100 ppm/¡ãC precision resistor to-ground on the board.
HDMI:a 499¦. (¡Â1% tolerance) resistor to-ground on the board

U3E

i.MX8M - CSI

MIPI_CSI1_CLK_N	A22	CSI_P1_CKN	CSI_P1_CKN	J7
MIPI_CSI1_CLK_P	B22	CSI_P1_CKP	CSI_P1_CKP	J7
MIPI_CSI1_D0_N	A23	CSI_P1_DN0	CSI_P1_DN0	J7
MIPI_CSI1_D0_P	B23	CSI_P1_DP0	CSI_P1_DP0	J7
MIPI_CSI1_D1_N	C22	CSI_P1_DN1	CSI_P1_DN1	J7
MIPI_CSI1_D1_P	D22	CSI_P1_DP1	CSI_P1_DP1	J7
MIPI_CSI1_D2_N	B24	CSI_P1_DN2	CSI_P1_DN2	J7
MIPI_CSI1_D2_P	C23	CSI_P1_DP2	CSI_P1_DP2	J7
MIPI_CSI1_D3_N	C21	CSI_P1_DN3	CSI_P1_DN3	J7
MIPI_CSI1_D3_P	D21	CSI_P1_DP3	CSI_P1_DP3	J7
MIPI_CSI2_CLK_N	A19	CSI_P2_CKN	CSI_P2_CKN	J5001
MIPI_CSI2_CLK_P	B19	CSI_P2_CKP	CSI_P2_CKP	J5001
MIPI_CSI2_D0_N	C20	CSI_P2_DN0	CSI_P2_DN0	J5001
MIPI_CSI2_D0_P	D20	CSI_P2_DP0	CSI_P2_DP0	J5001
MIPI_CSI2_D1_N	A20	CSI_P2_DN1	CSI_P2_DN1	J5001
MIPI_CSI2_D1_P	B20	CSI_P2_DP1	CSI_P2_DP1	J5001
MIPI_CSI2_D2_N	A21	CSI_P2_DN2	CSI_P2_DN2	J5001
MIPI_CSI2_D2_P	B21	CSI_P2_DP2	CSI_P2_DP2	J5001
MIPI_CSI2_D3_N	C19	CSI_P2_DN3	CSI_P2_DN3	J5001
MIPI_CSI2_D3_P	D19	CSI_P2_DP3	CSI_P2_DP3	J5001

CSI_P1_VDDIHA, CSI_P2_VDDIHA

MIMX8MQ6DVAJZAA
1.5GHz
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5V

U3C

i.MX8M - PCIe

PCIE1_TXN_N	J24	C196	100nF-ESL 25V	PCIE1_TXN	PCIE1_TXN WIFI MODULE
PCIE1_TXN_P	J25	C197	100nF-ESL 25V	PCIE1_TXP	PCIE1_TXP WIFI MODULE
PCIE1_RXN_N	H24			PCIE1_RXN	PCIE1_RXN WIFI MODULE
PCIE1_RXN_P	H25			PCIE1_RXP	PCIE1_RXP WIFI MODULE
PCIE1_REF_PAD_CLK_N	K24				
PCIE1_REF_PAD_CLK_P	K25				
PCIE1_RESREF	G25	R30	200 1%		GND
PCIE2_TXN_N	E24	C99	100nF 16V		J7
PCIE2_TXN_P	E25	C100	100nF 16V	PCIE2_TXP	PCIE2_TXP J7
PCIE2_RXN_N	D24	PCIE2_RXN			PCIE2_RXN J7
PCIE2_RXN_P	D25	PCIE2_RXP			PCIE2_RXP J7
PCIE2_REF_PAD_CLK_N	F24	PCIE2_REF_CLKM			
PCIE2_REF_PAD_CLK_P	F25	PCIE2_REF_CLKP			PCIE2_REF_CLKP CLOCK GENERATOR
PCIE2_RESREF	C25	R31	200 1%		GND

Change Capacitors

MIMX8MQ6DVAJZAA
1.5GHz
QUAD/COM

U3F

i.MX8M - HDMI

HDMI_DDC_SCL	R3	HDMI_DDC_SCL	HDMI_DDC_SCL	J7
HDMI_DDC_SDA	P3	HDMI_DDC_SDA	HDMI_DDC_SDA	J7
HDMI_HPD	W2	HDMI_HPD	HDMI_HPD	J7
HDMI_CEC	W3	HDMI_CEC	HDMI_CEC	J7

AC coupled differential low swing clock (HCSL levels)

HDMI_REFCLK_N	R1	HDMI_REFCLKN		
HDMI_REFCLK_P	R2	HDMI_REFCLKP		
HDMI_TX_M_LN_0	T2	CHDMI_TXN0	C198 100nF-ESL 25V	HDMI_TXN0 J7
HDMI_TX_P_LN_0	T1	CHDMI_TXP0	C199 100nF-ESL 25V	HDMI_TXP0 J7
HDMI_TX_M_LN_1	U1	CHDMI_TXN1	C200 100nF-ESL 25V	HDMI_TXN1 J7
HDMI_TX_P_LN_1	U2	CHDMI_TXP1	C179 100nF-ESL 25V	HDMI_TXP1 J7
HDMI_TX_M_LN_2	N1	CHDMI_TXN2	C180 100nF-ESL 25V	HDMI_TXN2 J7
HDMI_TX_P_LN_2	N2	CHDMI_TXP2	C201 100nF-ESL 25V	HDMI_TXP2 J7
HDMI_TX_M_LN_3	M2	CHDMI_TXN3	C202 100nF-ESL 25V	HDMI_CLKN J7
HDMI_TX_P_LN_3	M1	CHDMI_TXP3	C203 100nF-ESL 25V	HDMI_CLKP J7
HDMI_AUX_N	V2	CHDMI_AUXN	C204 100nF-ESL 25V	HDMI_AUXN J7
HDMI_AUX_P	V1	CHDMI_AUXP	C205 100nF-ESL 25V	HDMI_AUXP J7
HDMI_REXT	P1	R36	499 1%	GND

HDMI_AVDD1O

MIMX8MQ6DVAJZAA
1.5GHz
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R310 R311 R312 R313 R314 R315 R316 R317 — 604 1%

Q1A NX3020NAKS,115 (6, 2, 1)
Q1B NX3020NAKS,115 (3, 5, 4)

VDD_PHY_1V8

GND

HDMI_HPD — R35 5M1 — GND

U3D

i.MX8M - DSI

MIPI_DSI_CLK_N	C16	DSI_CKN	DSI_CKN	
MIPI_DSI_CLK_P	D16	DSI_CKP	DSI_CKP	
MIPI_DSI_D0_N	A17	DSI_DN0	DSI_DN0	
MIPI_DSI_D0_P	B17	DSI_DP0	DSI_DP0	
MIPI_DSI_D1_N	A16	DSI_DN1	DSI_DN1	
MIPI_DSI_D1_P	B16	DSI_DP1	DSI_DP1	
MIPI_DSI_D2_N	A18	DSI_DN2	DSI_DN2	
MIPI_DSI_D2_P	B18	DSI_DP2	DSI_DP2	
MIPI_DSI_D3_N	A15	DSI_DN3	DSI_DN3	
MIPI_DSI_D3_P	B15	DSI_DP3	DSI_DP3	
MIPI_DSI_REXT	C17	R34	15K 1%	GND

DSI_VDDIHA

MIMX8MQ6DVAJZAA
1.5GHz
QUAD/COM

U3B

i.MX8M - USB

USB1_VBUS	D14	USB1_VBUS	USB1_VBUS	
USB1_DN	B14	USB1_DN	USB1_DN	
USB1_DP	A14	USB1_DP	USB1_DP	
USB1_ID	C14	USB1_ID	USB1_ID	
USB1_TX_P	A13	USB1_TXP	USB1_TXP	
USB1_TX_N	B13	USB1_TXN	USB1_TXN	
USB1_RX_P	A12	USB1_RXP	USB1_RXP	
USB1_RX_N	B12	USB1_RXN	USB1_RXN	
USB1_RESREF	A11	R37	200 1%	GND
USB2_VBUS	D9	USB2_VBUS	USB2_VBUS	
USB2_DN	B10	USB2_DN	USB2_DN	
USB2_DP	A10	USB2_DP	USB2_DP	
USB2_ID	C9			
USB2_TX_P	A9	USB2_TXP	USB2_TXP	
USB2_TX_N	B9	USB2_TXN	USB2_TXN	
USB2_RX_P	A8	USB2_RXP	USB2_RXP	
USB2_RX_N	B8	USB2_RXN	USB2_RXN	
USB2_RESREF	B11	R40	200 1%	GND

USB_P0_VDD33, USB_P0_VPH, USB_P1_VDD33, USB_P1_VPH

MIMX8MQ6DVAJZAA
1.5GHz
QUAD/COM

VDD_3V3

R39 100K 1%

Y3 — 27MHZ 3.2x2.5 25PPM
OE (1), NC (2), GND (3), VCC (6), Q (4), Q̄ (5)

VDD_3V3

HDMI_REFCLKP, HDMI_REFCLKN

C101 100nF 16V

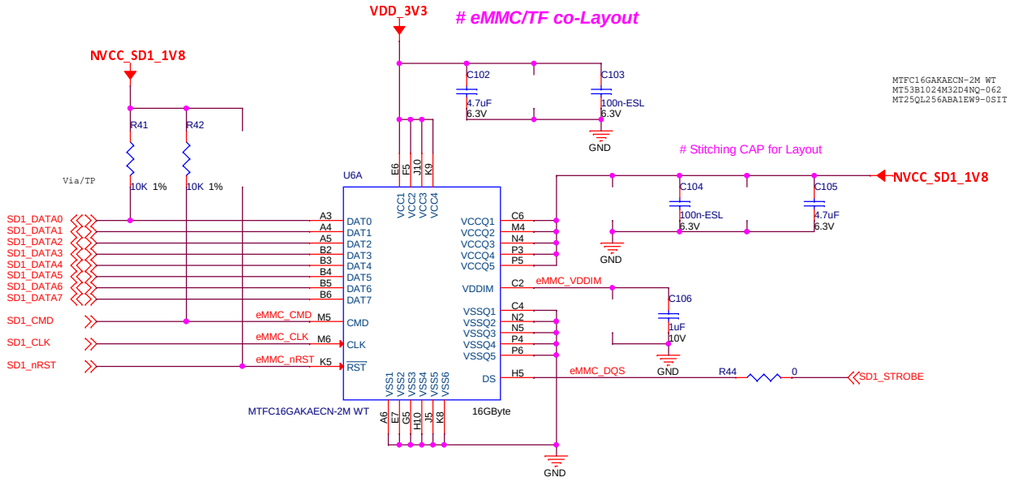
GND

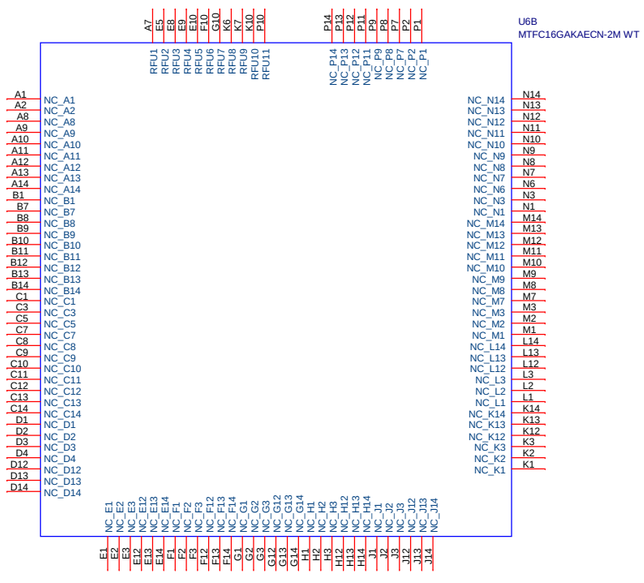
DIODES: NX5427001Z 5032 3.3V
AC coupled differential low swing clock (HCSL levels)

Size	Title	Rev
C	CPU PHY	1.0

Date: Thursday, October 18, 2018 Sheet 7 of 11

eMMC 5.0 Footprint

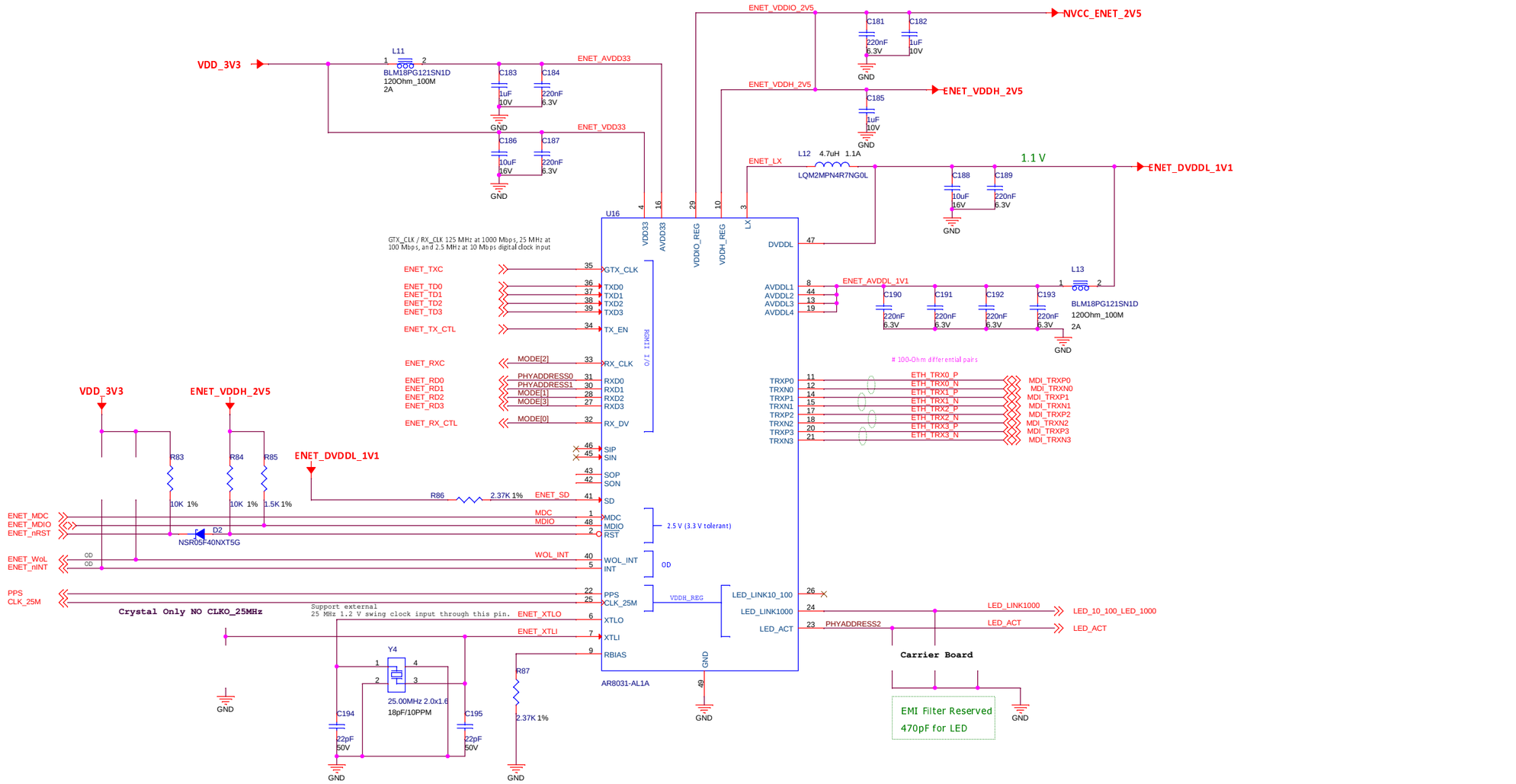




Size	Title	Rev
C	FLASH	1.0

Date: Wednesday, June 12, 2019 Sheet 8 of 11

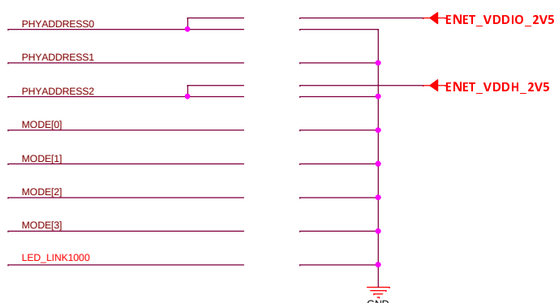
RGMII 10/100/1000 Ethernet

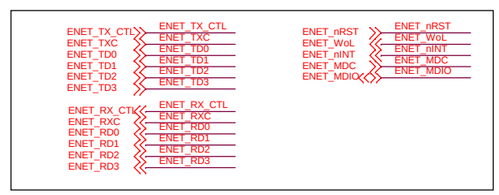


Power-on Strapping Pins

PHY PIN	PHY CFG	Default	Definition
RXD0	PHYADDRESS0	0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, 11b.
RXD1	PHYADDRESS1	0	
LED_ACT	PHYADDRESS2	1	
RX_DV	MODE[0]	0	0000 1000 Base-T, RGMII 0001 1000 Base-T, SGMII 0010 1000 Base-X, RGMII, 50Ω 0011 1000 Base-X, RGMII, 75Ω 0100 1000 Base-X/T, TRANS, 50Ω 0101 1000 Base-X/T, TRANS, 75Ω 0110 100 Base-FX, RGMII, 50Ω 0111 100 Base-FX/TX, TRANS, 50Ω 1001 RMII, copper/fiber auto-detection 1110 100 Base-FX, RGMII, 75Ω 1111 100 Base-FX/TX, TRANS, 75Ω Others Reserved
RXD2	MODE[1]	0	
RX_CLK	MODE[2]	0	
RXD3	MODE[3]	0	
LED_LINK1000	INT_SELECT	1	0: INT ; 1:GPIO

Power-on Strapping Pins CFG (Default)





Size	Title	Rev
C	ETHERNET	1.0

Date: Thursday, October 18, 2018 Sheet 11 of 11