

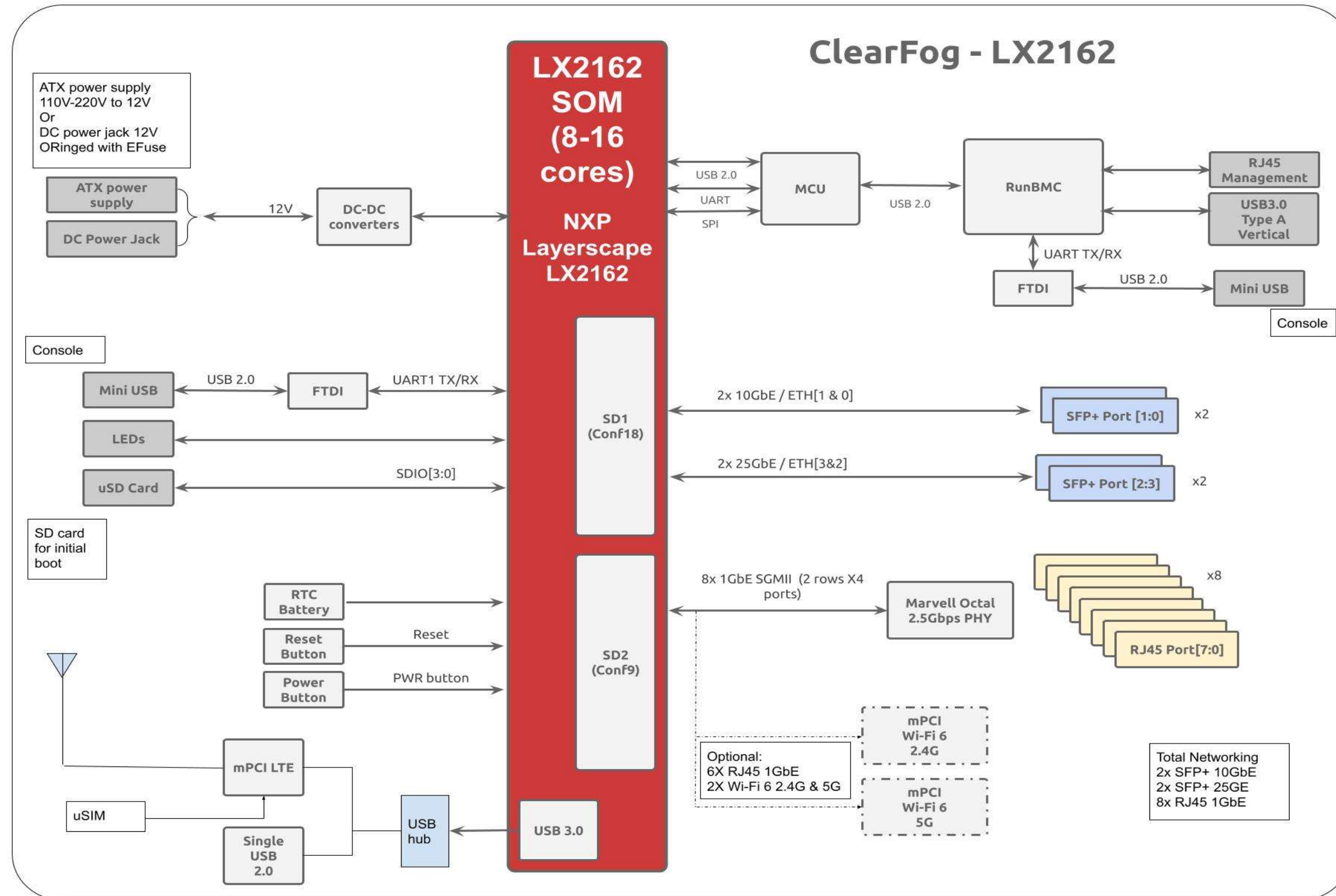
ClearFOG LX2162a
SolidRun Ltd.

Revision History

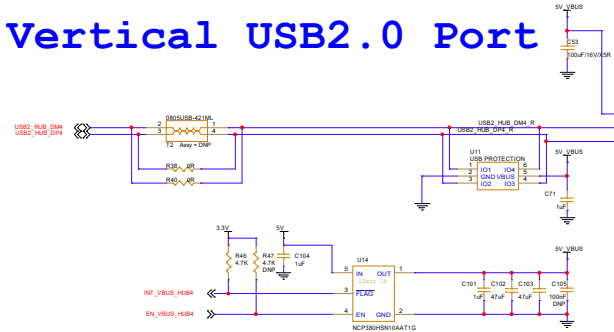
Rev#	Date	Owner	Description
1.0	Feb 2022	IlanB	First Release
1.1	Nov 2022	IlanB	Bug fix follow BU

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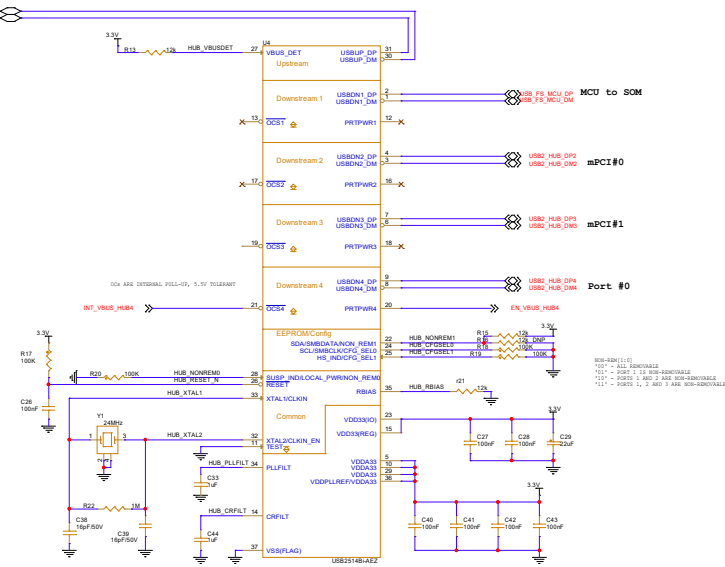
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3	RJ45 & PHY	8 port 1GE RJ45 and Marvel Octal PHY
4	Power	Power design
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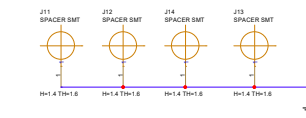
Vertical USB2.0 Port



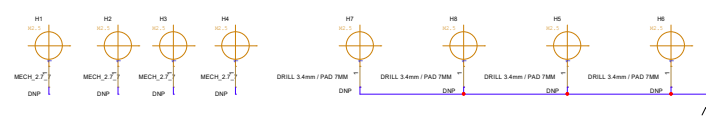
USB2.0 HUB



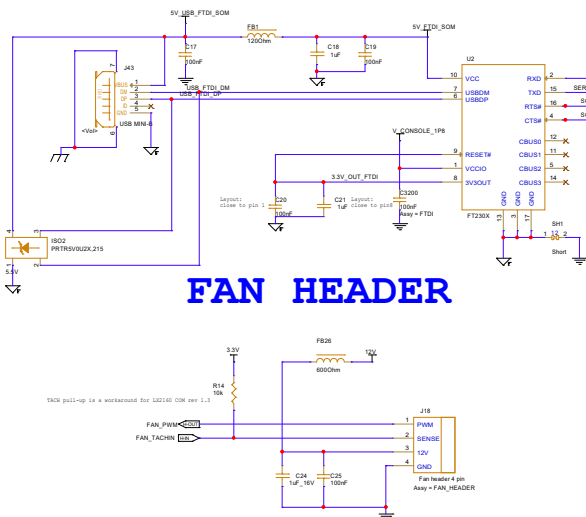
SOM Spacers



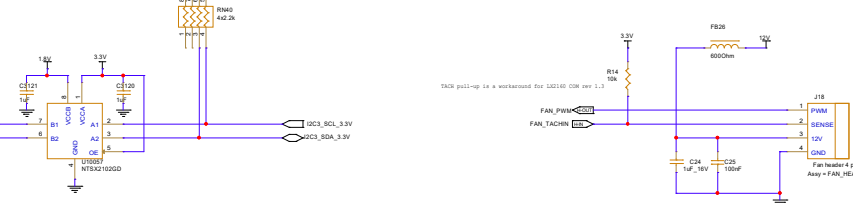
Mechanical Holes



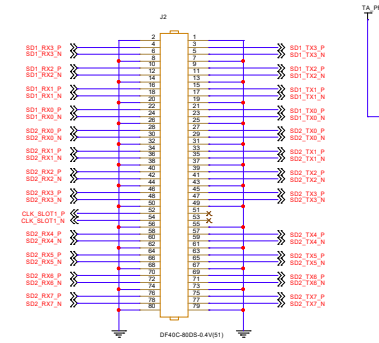
Onboard mUSB to Serial



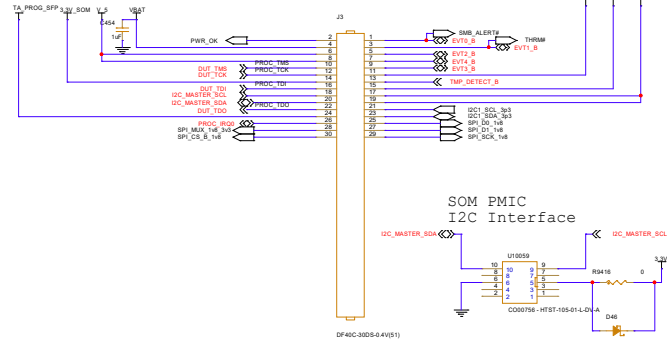
FAN HEADER



LX2162-SOM Interface



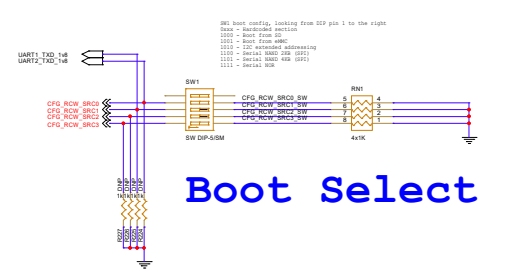
SOM PMIC I2C Interface



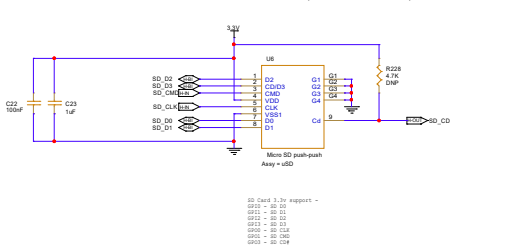
JTAG



Boot Select

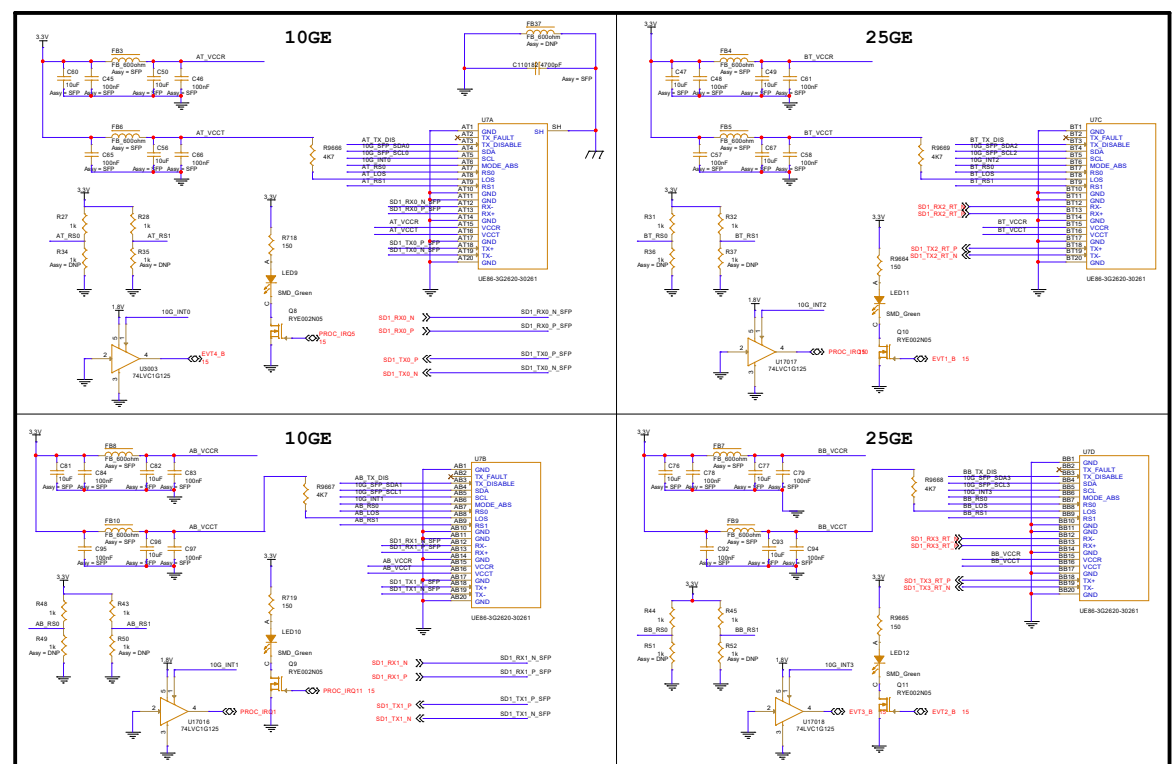
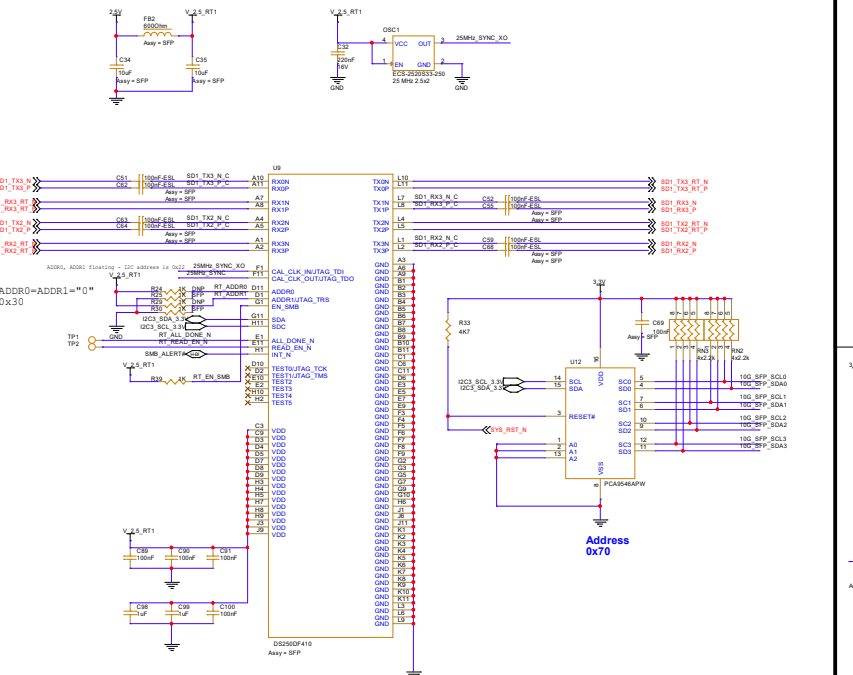


micro SD connector (bootable)

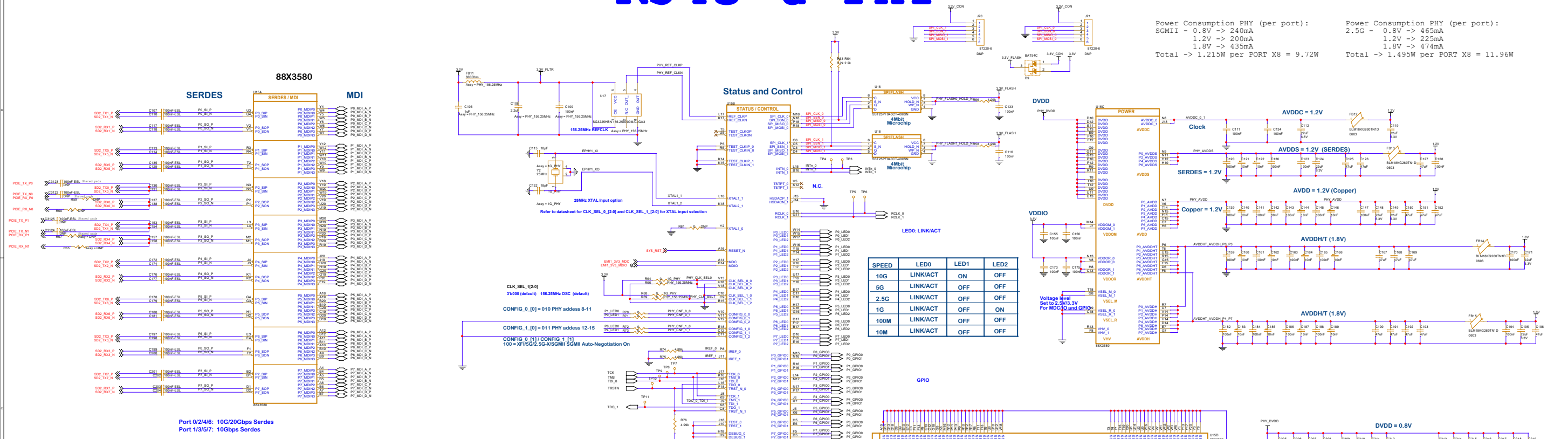


History Revision	
1.0	First Release
1.1	Bug fix after BU

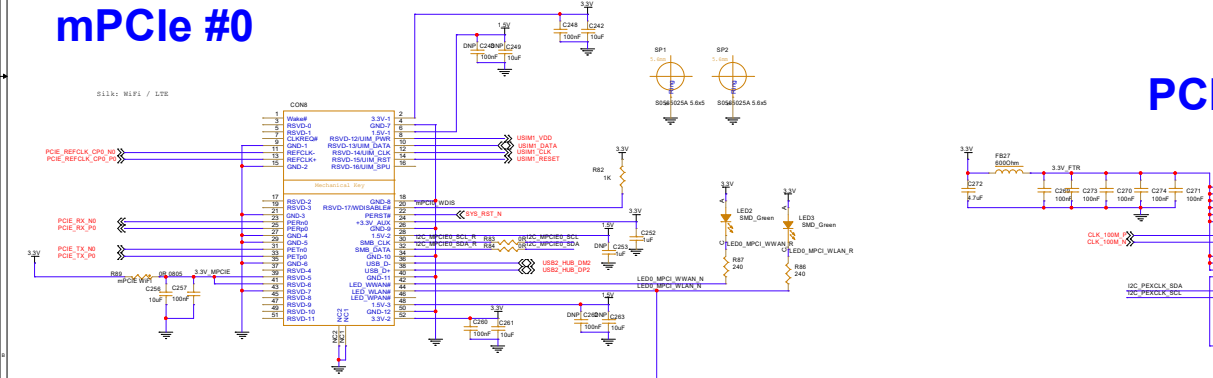
SFPs



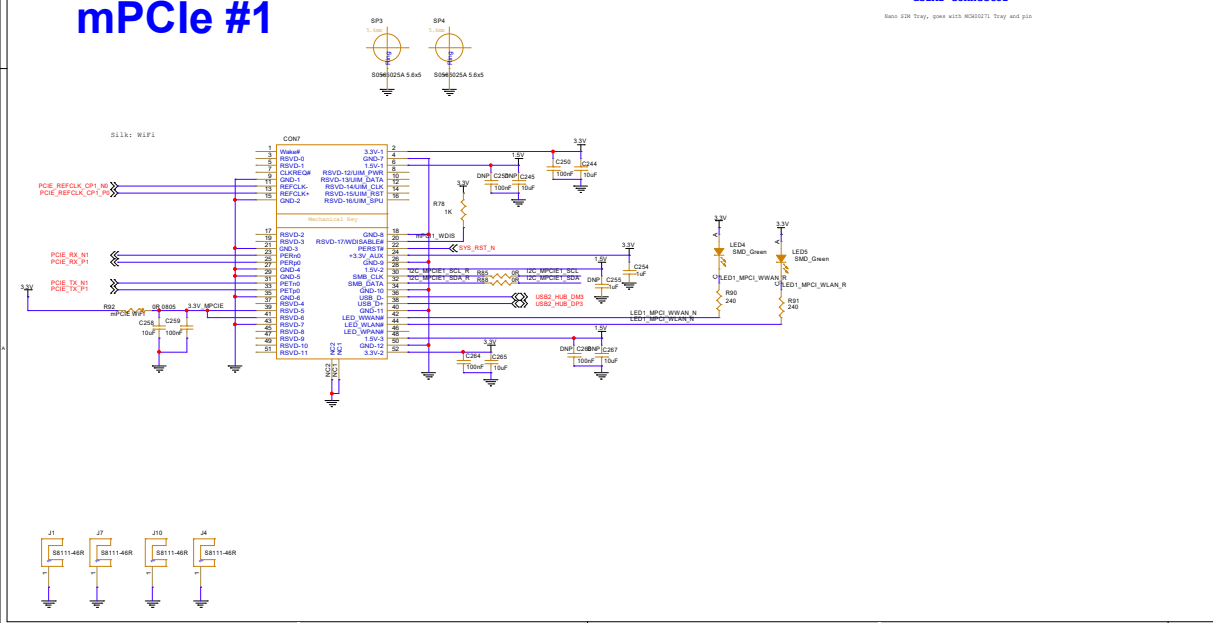
RJ45 & PHY



PCIe X1 Gen3 802.11ac wave2 or LTE 4G mPCIe #0



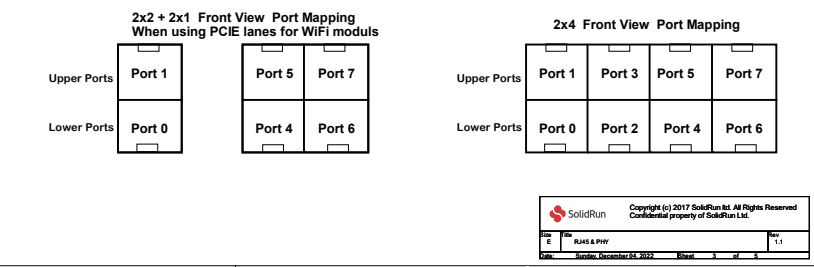
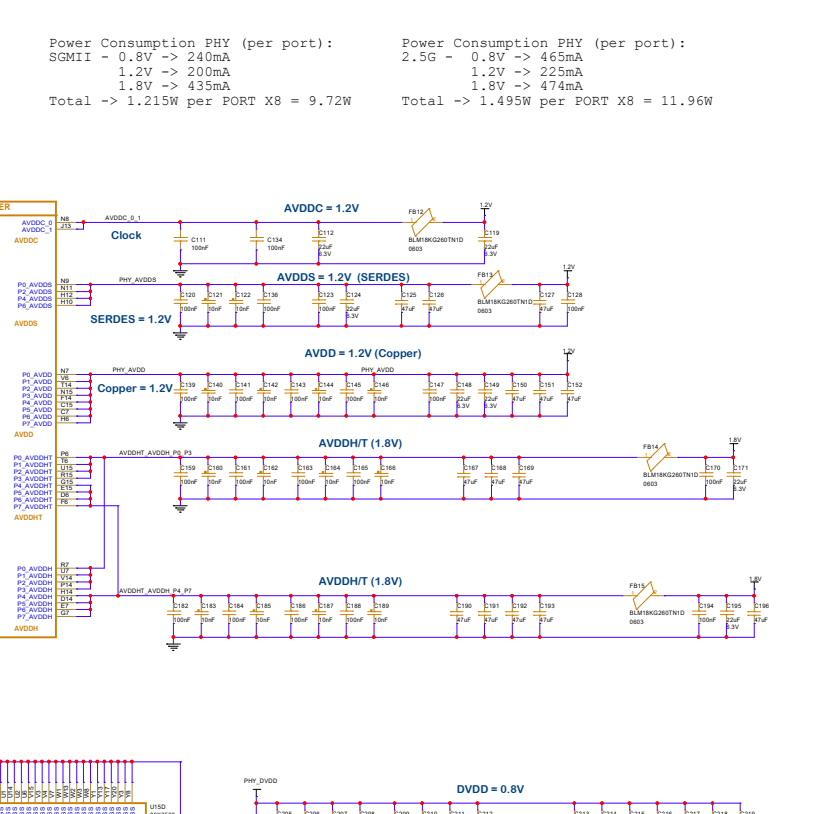
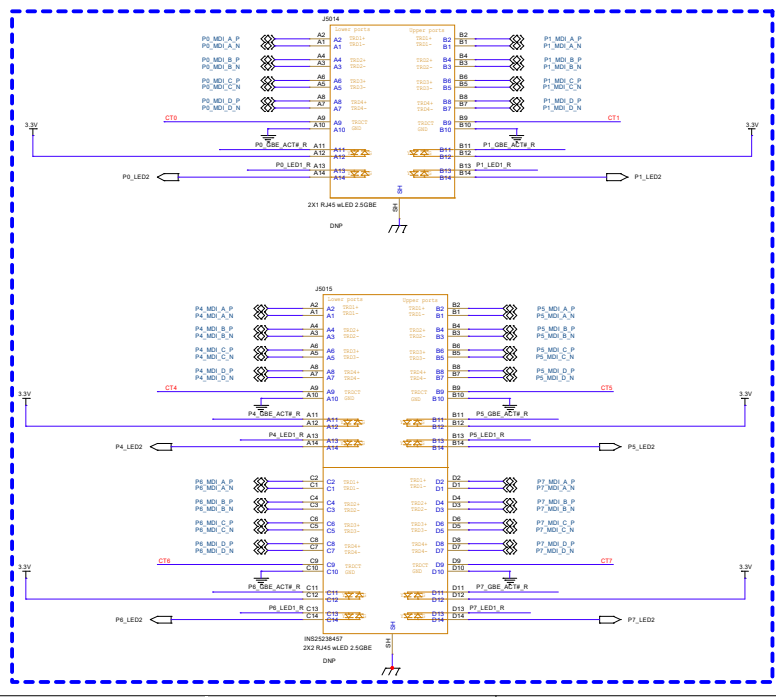
PCIe X1 Gen3 802.11ac wave2 mPCIe #1



PCIe Clock

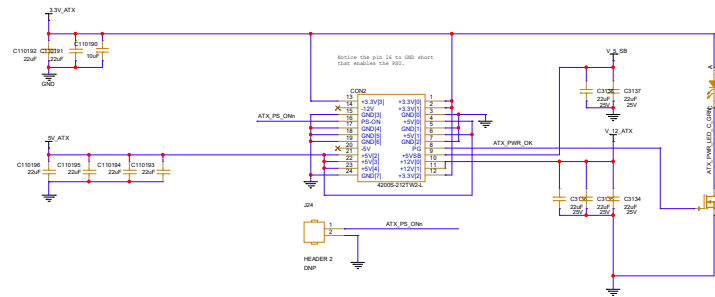


Assemble only when using PCIE lane for WiFi

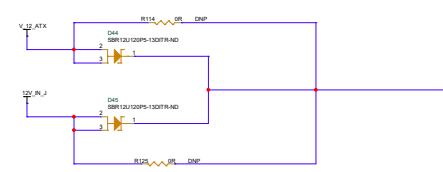


POWER

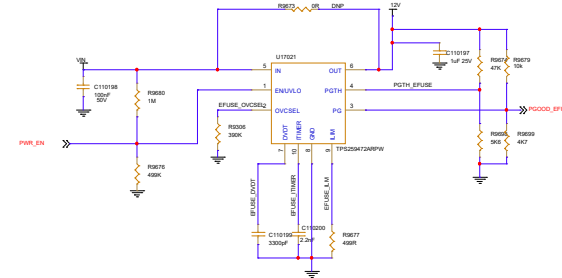
ATX PSU connector



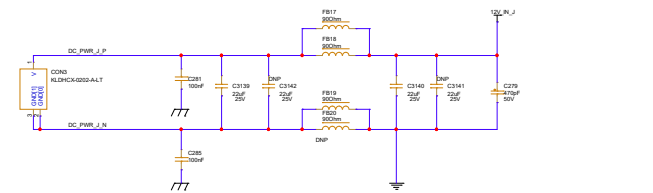
12V ORing



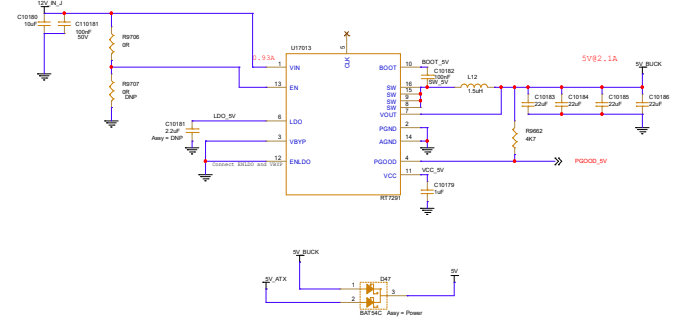
E Fuse



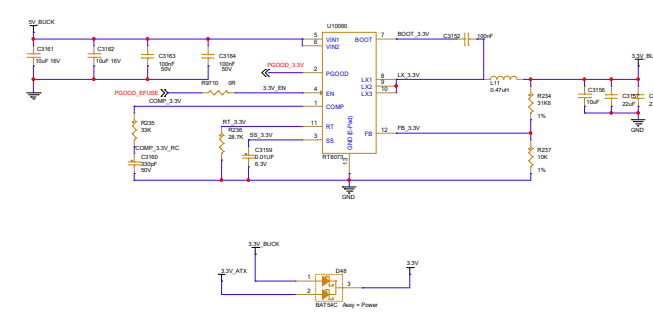
DC Power Jack



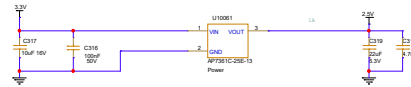
5V



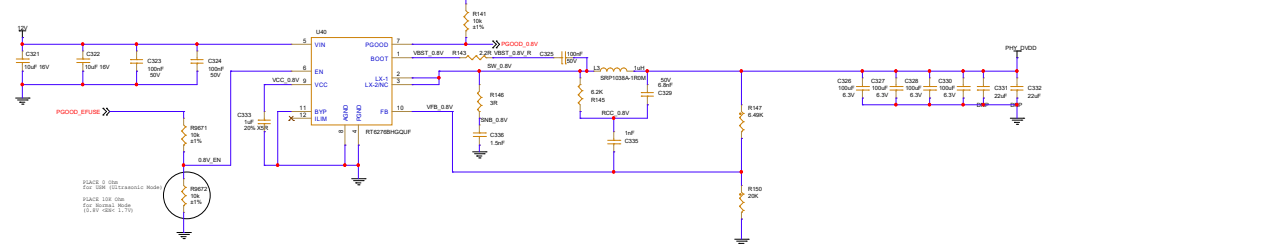
3.3V



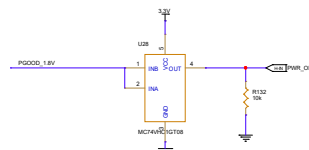
2.5V



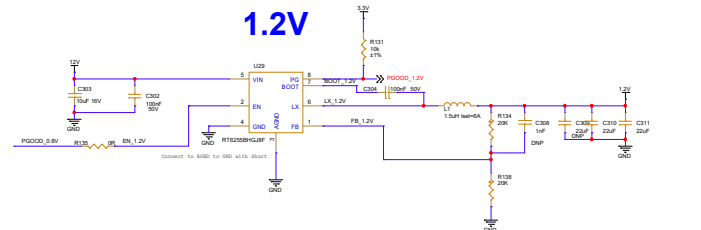
0.8V



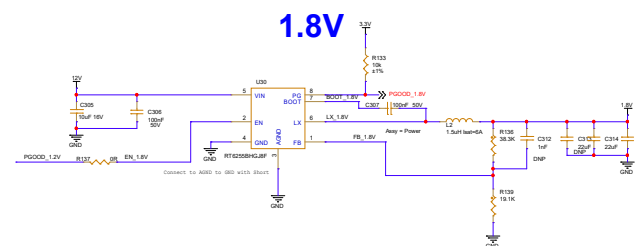
Power OK to SOM



1.2V



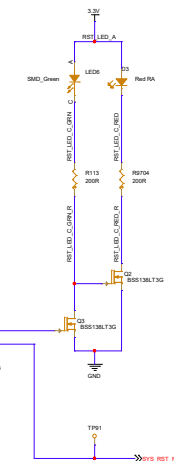
1.8V



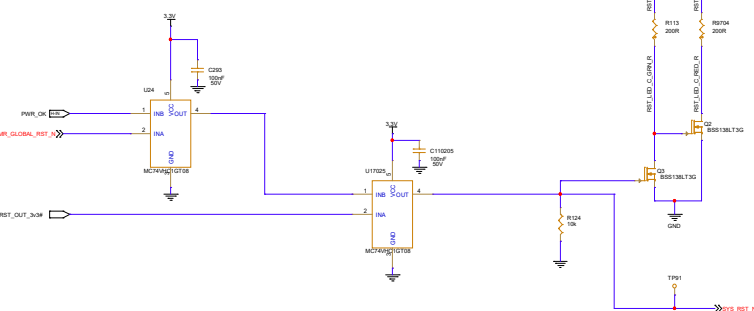
1.5V



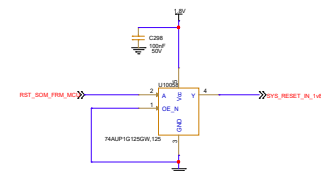
Reset LEDs



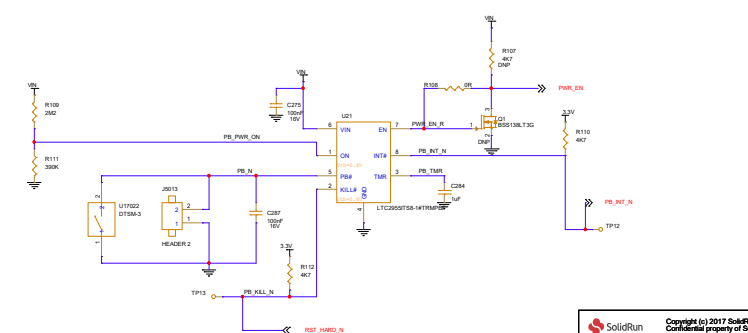
Reset



Reset SOM from MCU



Power push button



RUNBMC

MCU

MCU FILTERS

Diagram showing the connection of pins 1 to 5 of the 705430039 component to the system power and data bus:

- Pin 1: I2C_BMC_SDA
- Pin 2: I2C_BMC_SCL
- Pin 3: ATX_PWR_EN
- Pin 4: GND
- Pin 5: NC

VGA

Connector Standard: BMC daughter board I/O specification
Rev1.4.1 and MO-310C