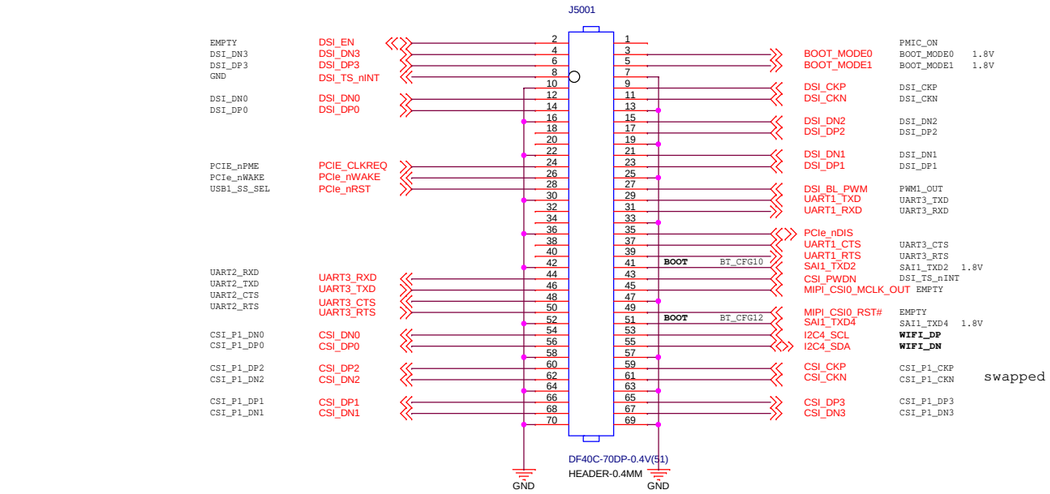
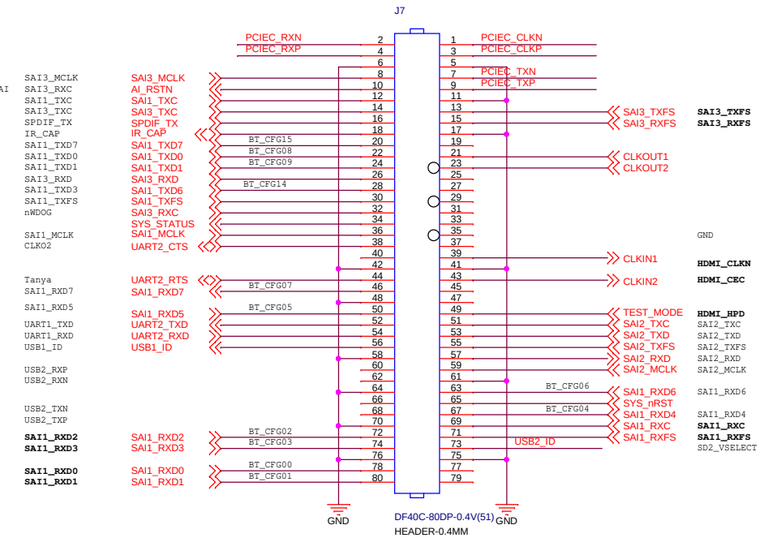
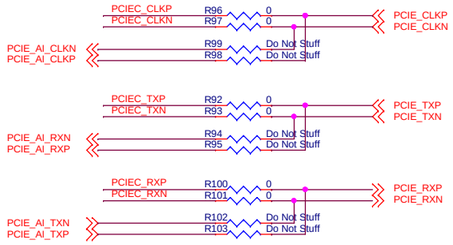
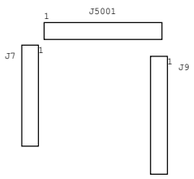


swapped

Mini_PCIe reset same as AI

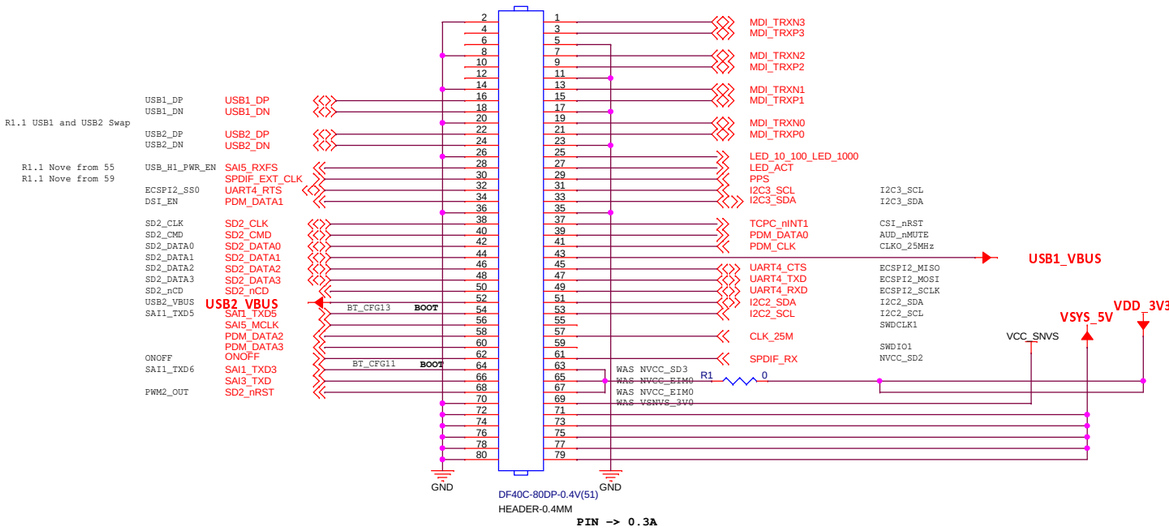






R1.1 USB1 and USB2 Swap

R1.1 Nove from 55
R1.1 Nove from 59



PIN -> 0.3A

SRMM8QDW00D02GE008V12C0 nA nW

Size	Title	Rev
C	B-T-B CONNECTORS	1.2
Date: Monday, January 06, 2020	Sheet 1 of 12	

ETHERNET PHY

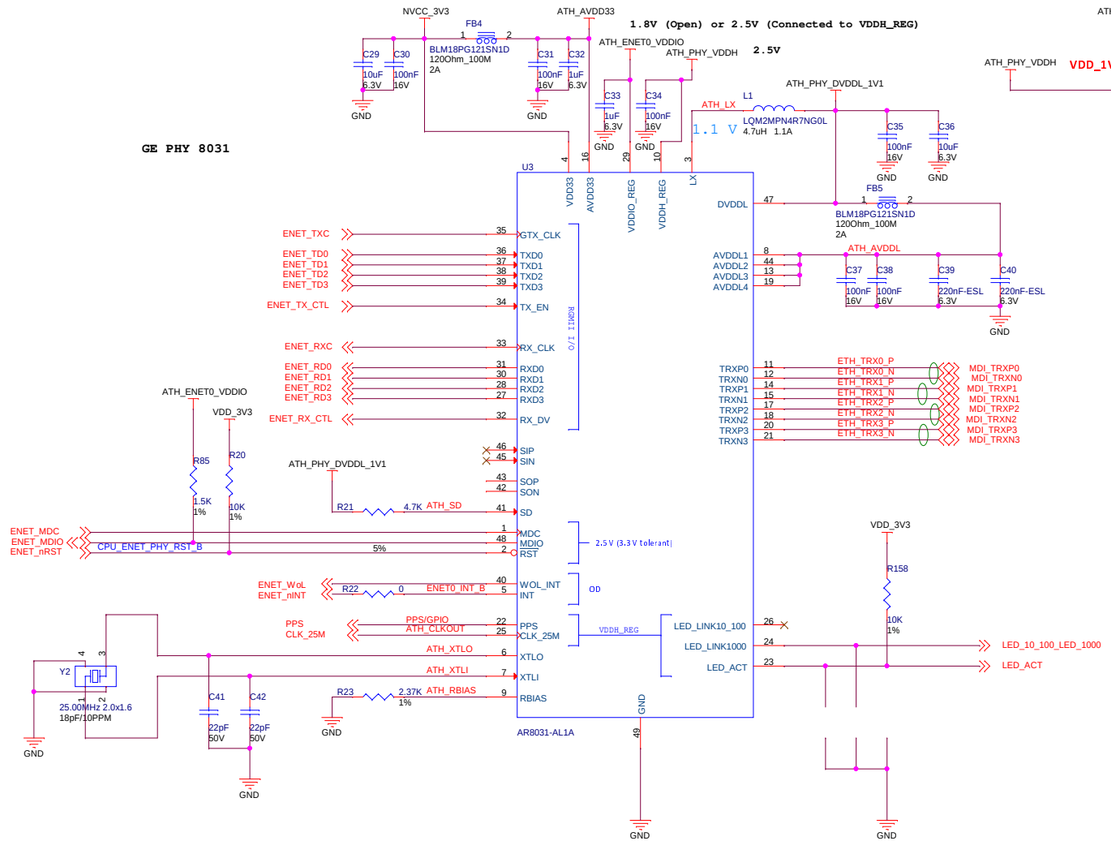
MODE2[3:0]

(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved

Power-on Strapping Pins

PHYADDRESS0 — ENET0_RGMII_RXD0
PHYADDRESS1 — ENET0_RGMII_RXD1
MODE2[1] — ENET0_RGMII_RXD2
MODE2[3] — ENET0_RGMII_RXD3
MODE2[2] — ENET0_RGMII_RXC
MODE2[0] — ENET0_RGMII_RX_CTL
SEL_GPIO_INT (0: INT ; 1:GPIO) — LED_1000
ANA_MOD (Select the core voltage level: 0:1.1V, 1:1.2V) — LED_ACT

GE PHY 8031



Power-on Strapping Pins

PHY PIN	PHY CFG	Default	Definition
RXD0	PHYADDRESS0	0	LED_ACT and RXD1-0 set the lower three bits of the physical address. The upper two bits of the physical address are set to the default, 1'b00.
RXD1	PHYADDRESS1	0	
LED_ACT	PHYADDRESS2	1	
RX_DV	MODE[0]	0	0000 1000 Base-T, RGMII; 0001 1000 Base-T, SGMII; 0010 1000 Base-X, RGMII, 50 Ω; 0011 1000 Base-X, RGMII, 75 Ω; 0100 1000 Base-X/T, TRANS, 50 Ω; 0101 1000 Base-X/T, TRANS, 75 Ω; 0110 100 Base-FX, RGMII, 50 Ω; 0111 100 Base-FX/TX, TRANS, 50 Ω; 1011 RMII, copper/fiber auto-detection; 1100 100 Base-FX, RGMII, 75 Ω; 1111 100 Base-FX/TX, TRANS, 75 Ω; Others Reserved.
RXD2	MODE[1]	0	
RX_CLK	MODE[2]	0	
RXD3	MODE[3]	0	
LED_LINK1000	INT_SELECT	1	0: INT ; 1:GPIO

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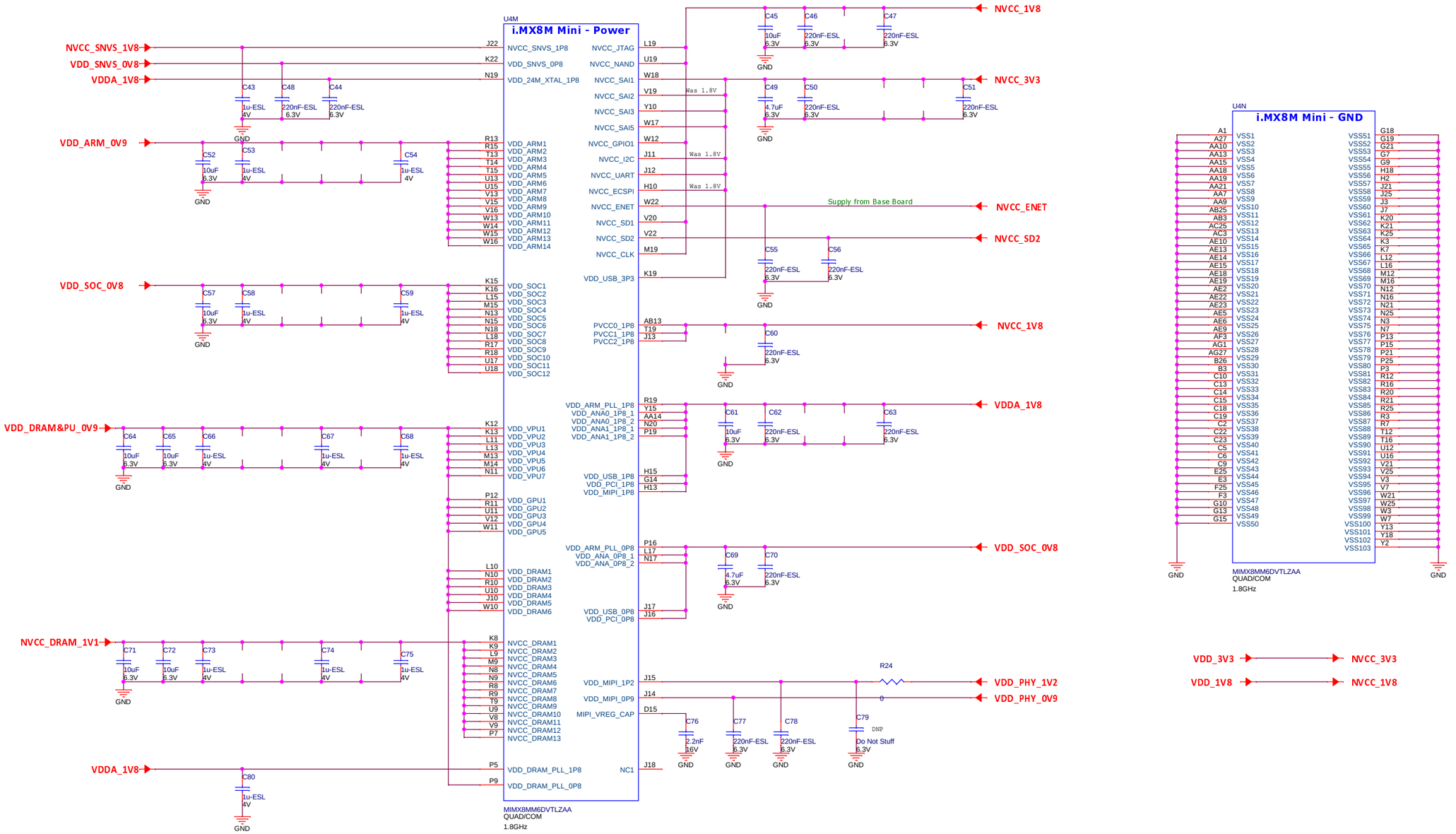
Size	Title	Rev
A2	ETHERNET_PHY	1.2

Date: Monday, January 06, 2020 Sheet 3 of 12

i.MX8M Mini PWR

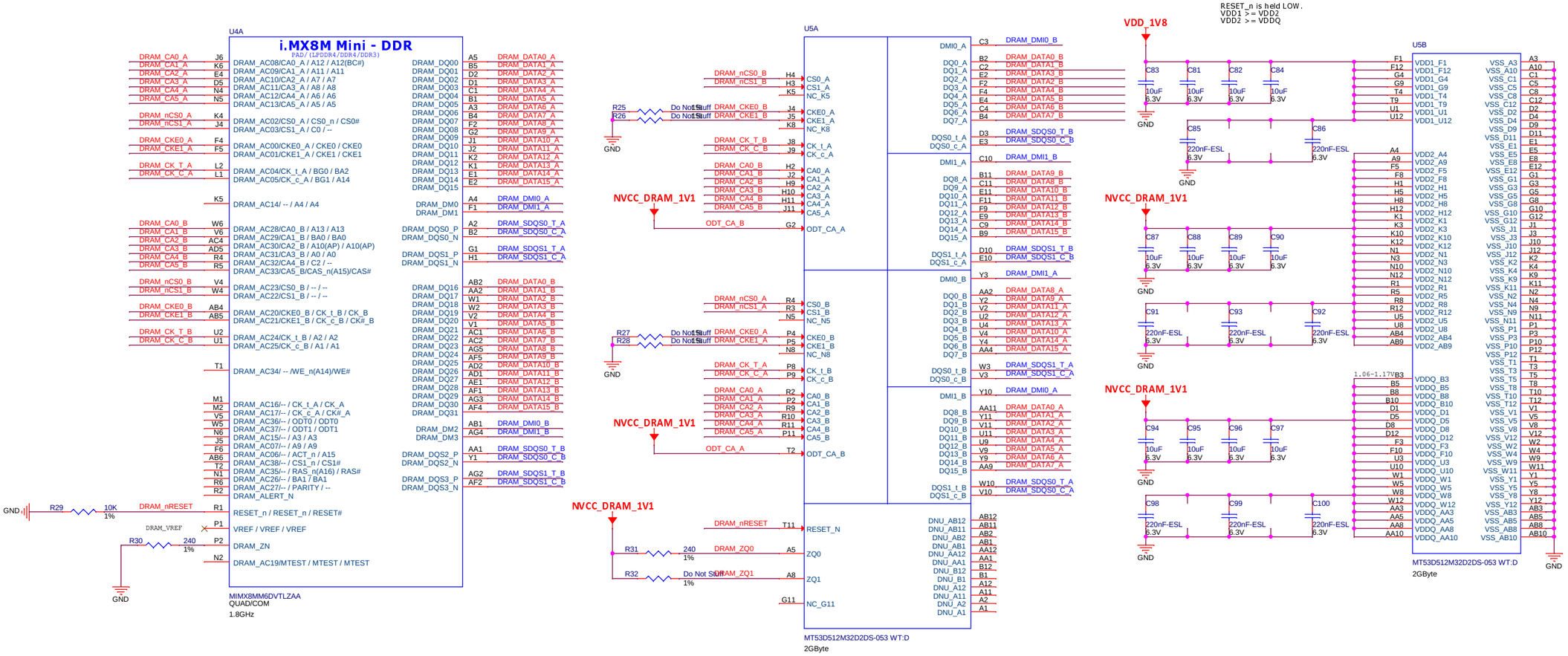


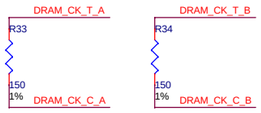
SRMM8QDW00D02GE008V12C0 nA nW

Size	Title	Rev
C	CPU PWR	1.2

Date: Monday, January 06, 2020 Sheet 4 of 12

LPDDR4 2GB





Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A
DRAM_DQ00	DQ0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A
DRAM_DQ07	DQ7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A
DRAM_DQ08	DQ8_A	DQU0_A
DRAM_DQ09	DQ9_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B
DRAM_DQ16	DQ0_B	DQL0_B
DRAM_DQ17	DQ1_B	DQL1_B
DRAM_DQ18	DQ2_B	DQL2_B
DRAM_DQ19	DQ3_B	DQL3_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ21	DQ5_B	DQL5_B
DRAM_DQ22	DQ6_B	DQL6_B
DRAM_DQ23	DQ7_B	DQL7_B
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B
DRAM_DQ24	DQ08_B	DQU0_B
DRAM_DQ25	DQ09_B	DQU1_B
DRAM_DQ26	DQ10_B	DQU2_B
DRAM_DQ27	DQ11_B	DQU3_B
DRAM_DQ28	DQ12_B	DQU4_B
DRAM_DQ29	DQ13_B	DQU5_B
DRAM_DQ30	DQ14_B	DQU6_B
DRAM_DQ31	DQ15_B	DQU7_B

Command/Address

Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	/	ACT_n
DRAM_AC07	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14		A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC18	/	/
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS1_B	/
DRAM_AC23	CS0_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34		WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_AC39	/	C1
DRAM_ZN_SENSE	ZQ	ZQ
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

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Size	Title	Rev
C	LPDDR4	1.2

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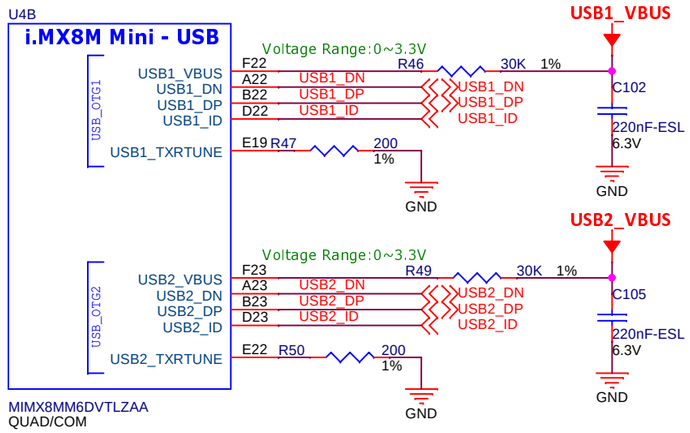
i.MX8M Mini IO Interface

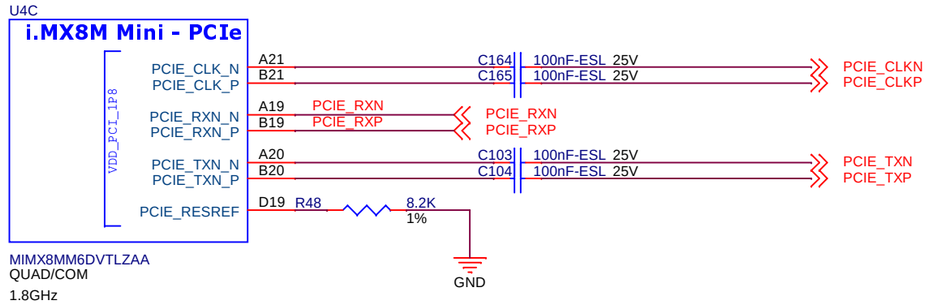
SRMM8QDW00D02GE008V12C0 nA nW

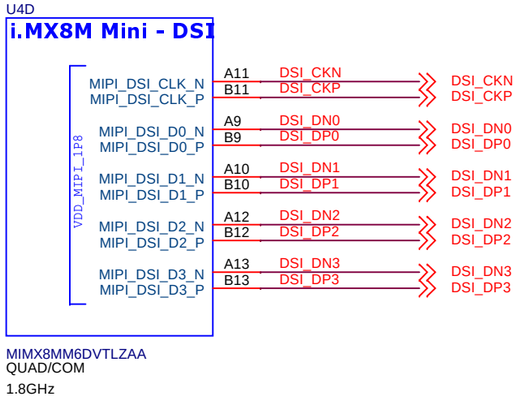
Size	Title	Rev
C	CPU IO	1.2

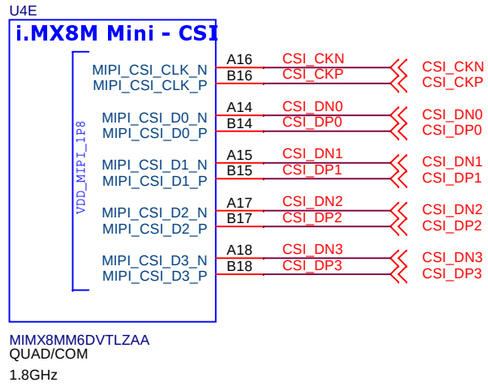
Date: Monday, January 06, 2020 Sheet 6 of 12

i.MX8M Mini PHYs









SRMM8QDW00D02GE008V12C0 nA nW

Size	Title	Rev
B	CPU PHY	1.2

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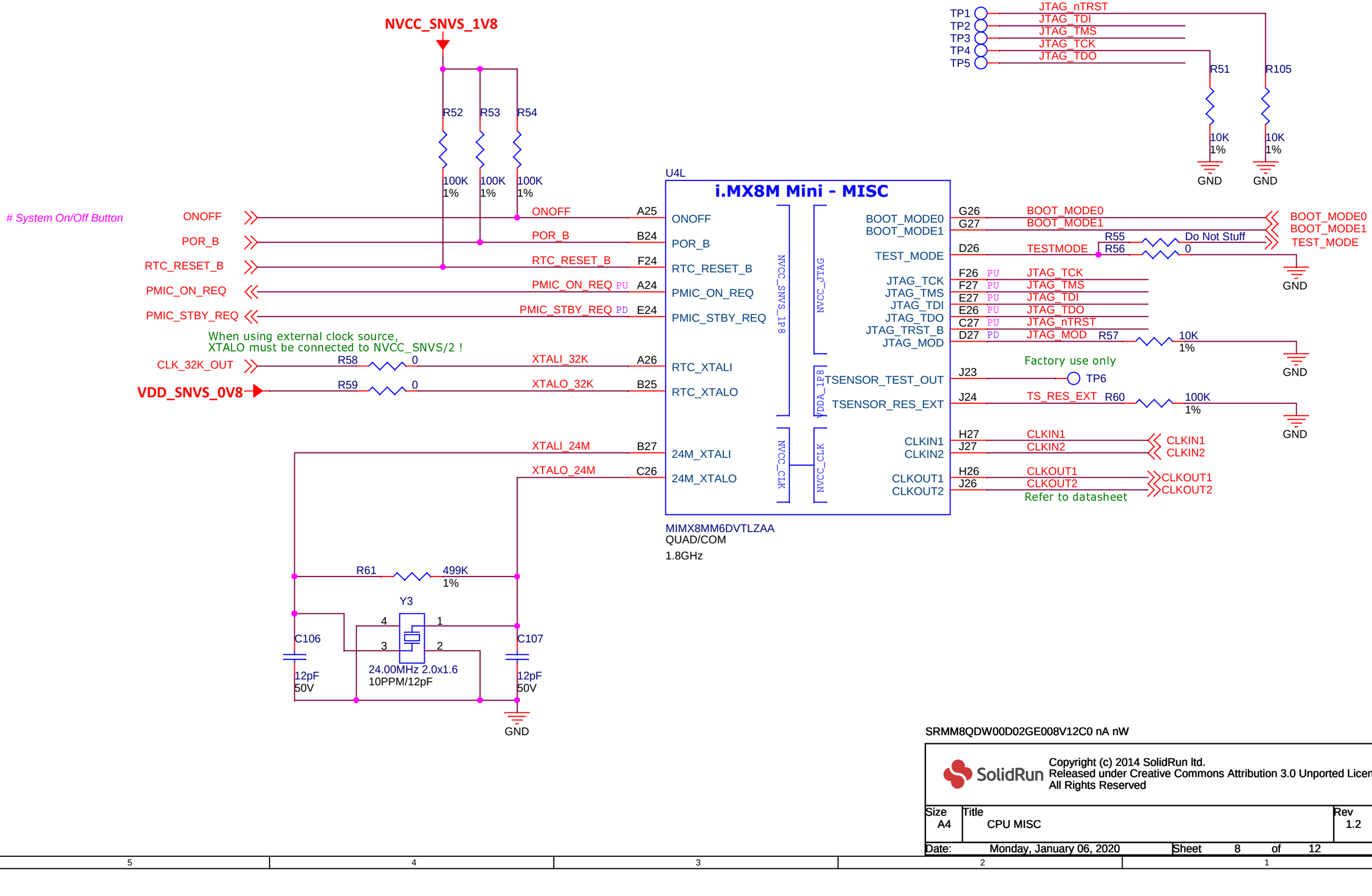
i.MX8M Mini MISC

JTAG Debug



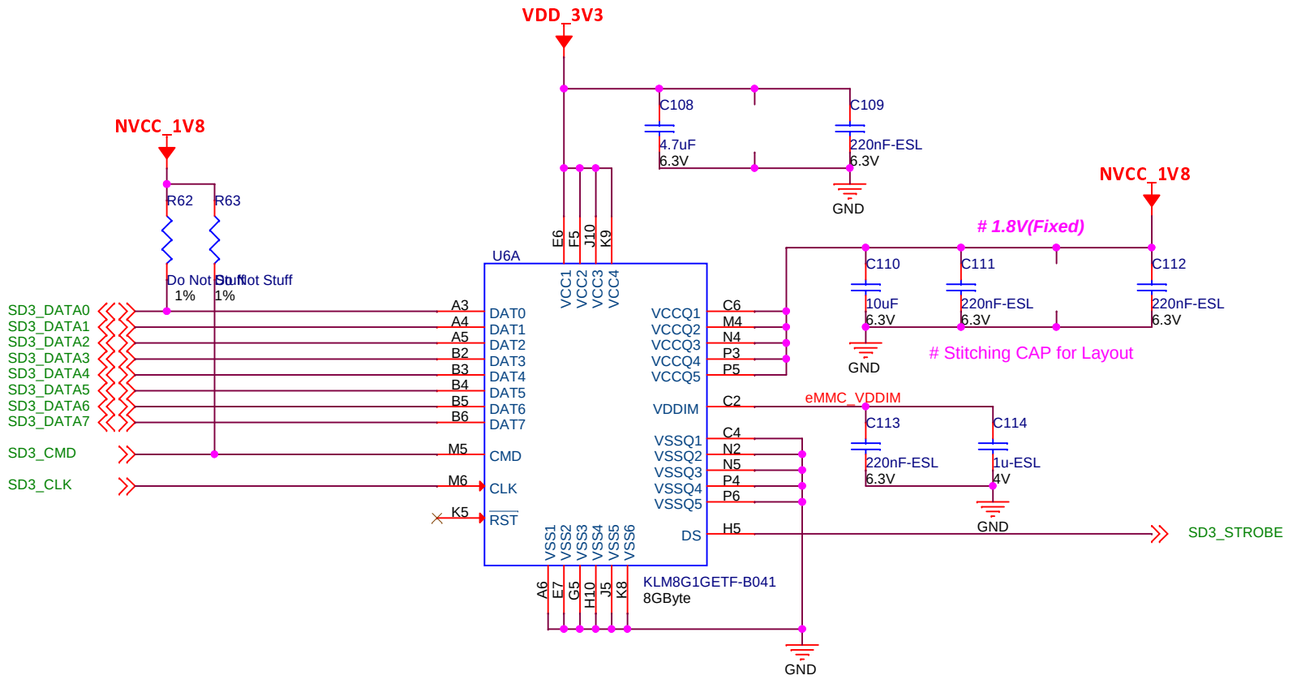
SRMM8QDW00D02GE008V12C0 nA nW

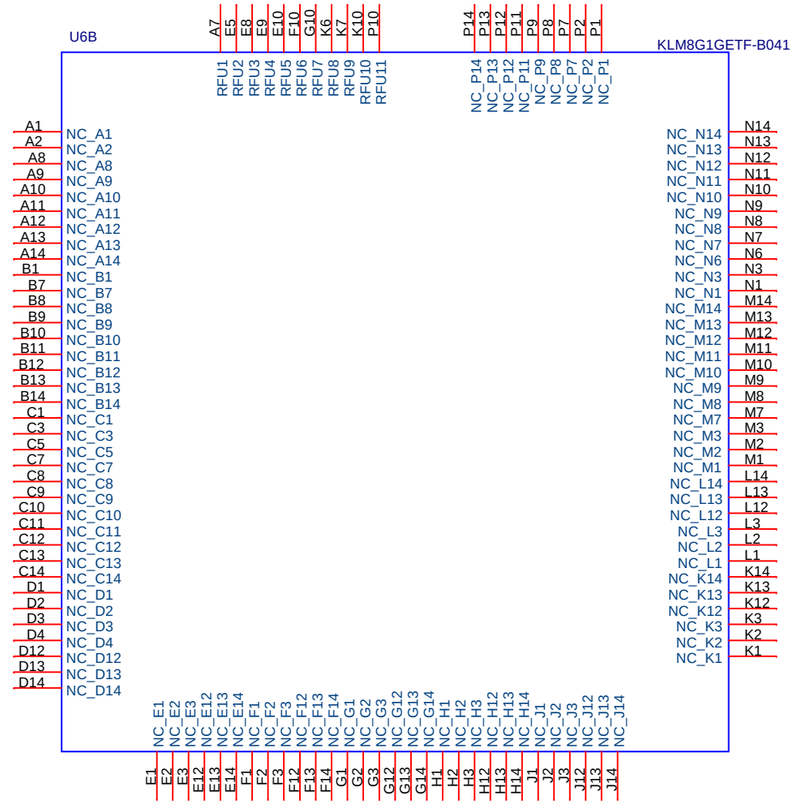
Size	Title	Rev
A4	CPU MISC	1.2

Date: Monday, January 06, 2020 Sheet 8 of 12

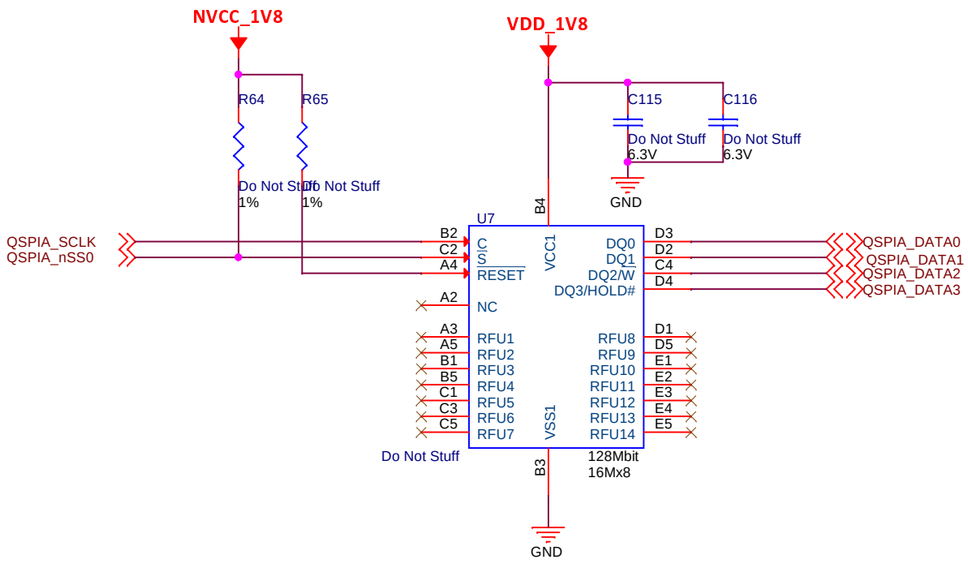
Storage

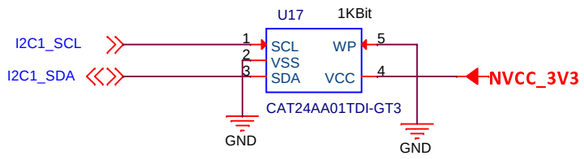
eMMC 5.1





QSPI Flash





SRMM8QDW00D02GE008V12C0 nA nW

Size	Title	Rev
B	eMMC/QSPI	1.2

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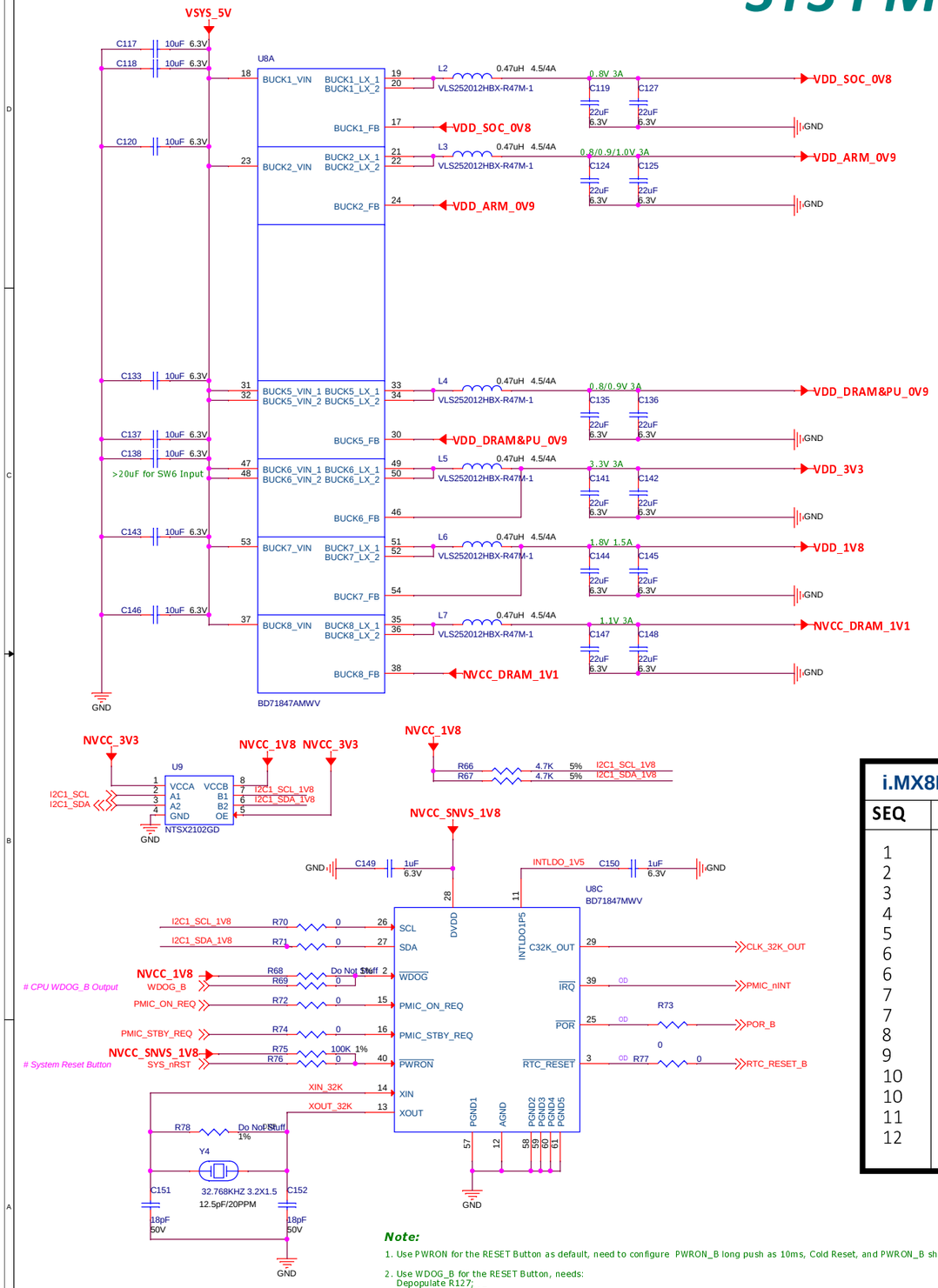
SYS PMIC



i.MX8M Mini LPDDR4 EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Curr(mA)
1	NVCC_SNVS_1V8	LDO1	1.65	1.8	1.95	10
2	VDD_SNVS_0V8	LDO2	0.81	0.8	0.89/0.945	10
3	RTC_RESET_B	RTC_RESET_B	--	--	--	--
4	CLK_32K_OUT	RTC_CLK	--	--	--	--
5	VDD_SOC_0V8	BUCK1	0.72	0.8	0.88	3000
6	VDD_DRAM&PU_0V9	BUCK5	0.72/0.81	0.8/0.9	0.88/0.945	3000
6	VDD_PHY_0V9	LDO4	0.81	0.9	0.945	250
7	VDD_ARM_0V9	BUCK2	0.72/0.81/0.9	0.8/0.9/1.0	0.88/0.945/1.025	3000
7	VDDA_1V8	LDO3	1.71	1.8	1.89	300
8	VDD_1V8/NVCC_1V8	BUCK7	1.65	1.8	1.95	1500
9	NVCC_DRAM_1V1	BUCK8	1.045	1.1	3.6	3000
10	NVCC_3V3	BUCK6	3	3.3	3.6	3000
10	NVCC_SD2	MUXSW	3.0/1.65	3.3/1.8	1.155	150
11	VDD_PHY_1V2	LDO6	1.14	1.2	1.26	300
12	POR_B	POR_B	--	--	--	--

Note:

1. Use PWRON for the RESET Button as default, need to configure PWRON_B long push as 10ms, Cold Reset, and PWRON_B short push detect should be disabled !
2. Use WDOG_B for the RESET Button, needs:
   Depopulate R127;
   Populate R128, R107;
   Configure WDOG_B as Cold Reset!

SRMM8QDW00D02GE008V12C0 nA nW

Size	Title	Rev
C	PMIC	1.2

Date: Monday, January 06, 2020 Sheet 11 of 12

Rev. 1.0	Prototype Version
Rev. 1.1	1. Swapping USB1 and USB2 in J9 2. Changing U10 Vin fro 3.3V to 5V 3. Adding R86 (1M) and R87 (10) for AI's Crystal 4. Adding 1KBit EEPROM 5. Move SPDIF_EXT_CLK from pin 59 to pin 30 6. Move SAI5_RXFS from pin 55 to pin 28 to support USB_PWR_EN 7. Adding SWDIO1 and SWDCLK1 to support NINA-B flashing 8. Adding an assembly option to connect the AI chip to the PCIe 9. Adding Pull-Down on JTAG_nTRST (R105) to enable IMX8M-Nano booting
Rev. 1.2	1. AI chip is connected using the PCIe interface only. 2. Replacing the WI-Fi to Murata's LBEE5HY1MW-230. 3. Changing R20 to 10K and marking it as DNU 4. Changing R80 to 2.49K (VDD09 = 1.0V). 5. Adding C249, 22uF capacitor to VDD0.9V . 6. Adding R157, 0 OHM, to add optional connection of 2.5V to NVCC_ENET 7. Adding R158, 10K, pull-up to support active low led activity 8. R45 is DNU enable uSD card power during Boot

SRMM8QDW00D02GE008V12C0 nA nW

Size	Title	Rev
A	Version History	1.2

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