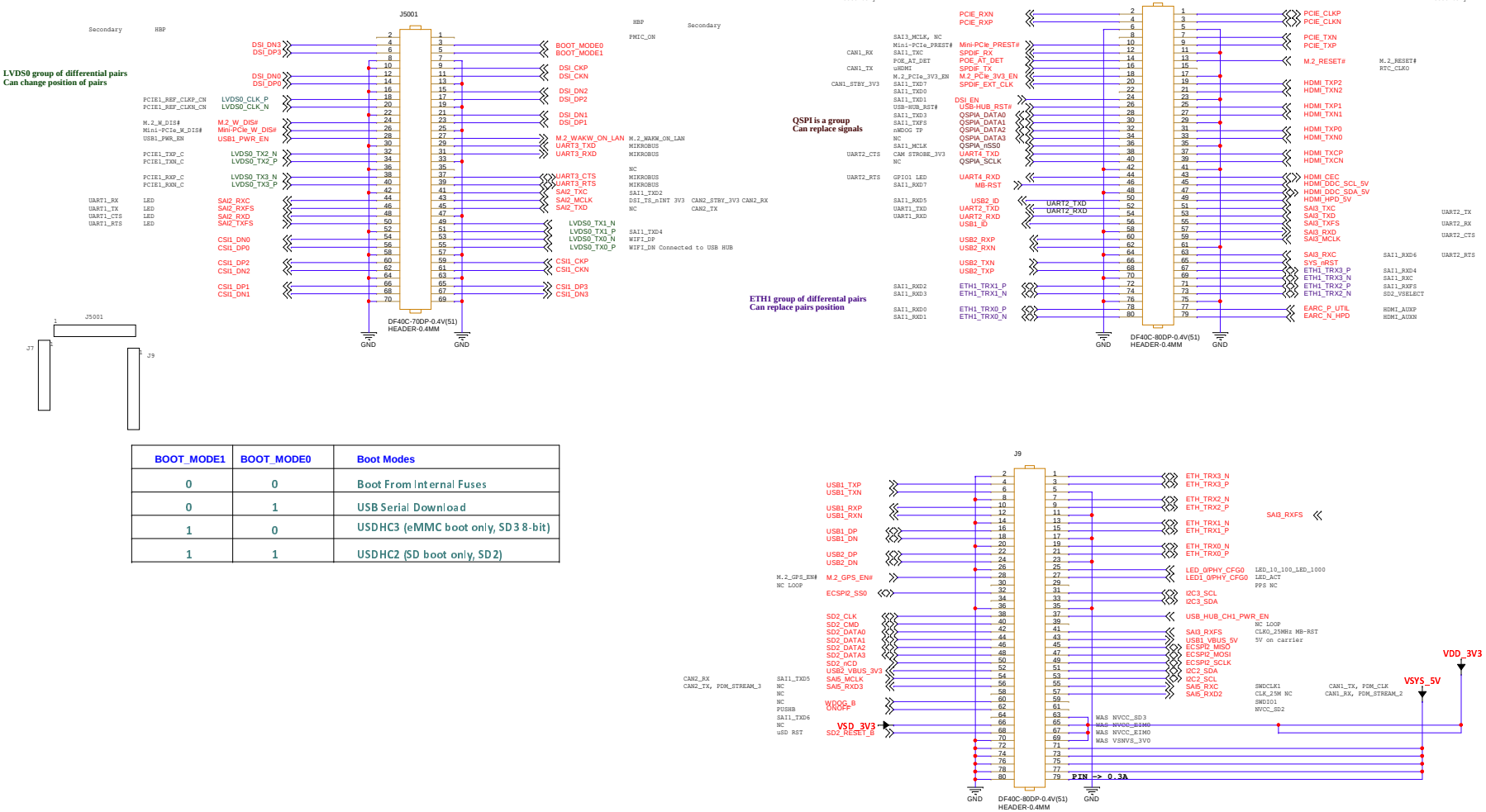


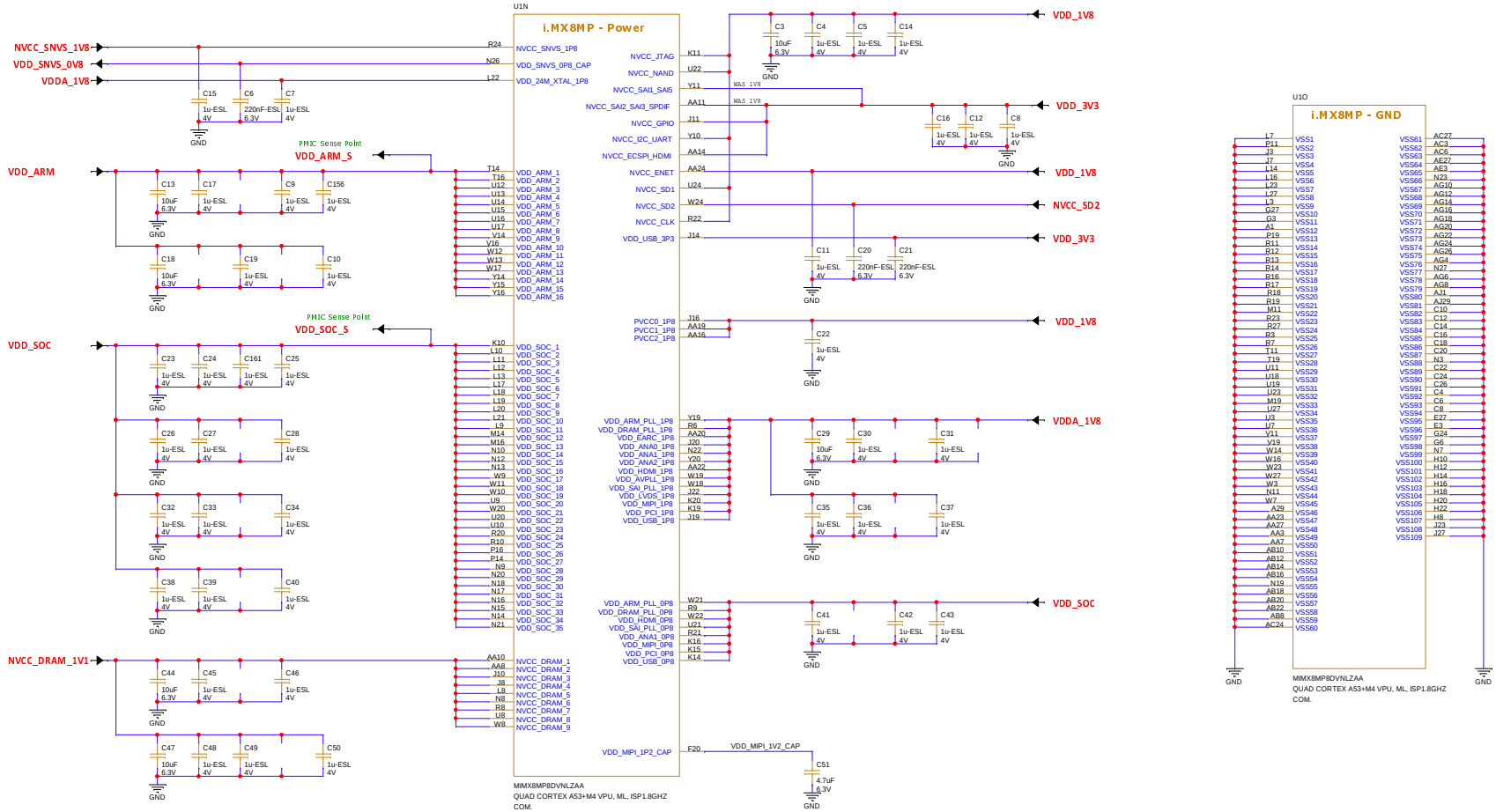
BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	Boot From Internal Fuses
0	1	USB Serial Download
1	0	USDHC3 (eMMC boot only, SD3 8-bit)
1	1	USDHC2 (SD boot only, SD2)

Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

Size	Title	Rev
C	B-T-B CONNECTORS	1.1

Date: Tuesday, October 03, 2023 Sheet 1 of 11

i.MX8M Plus PWR

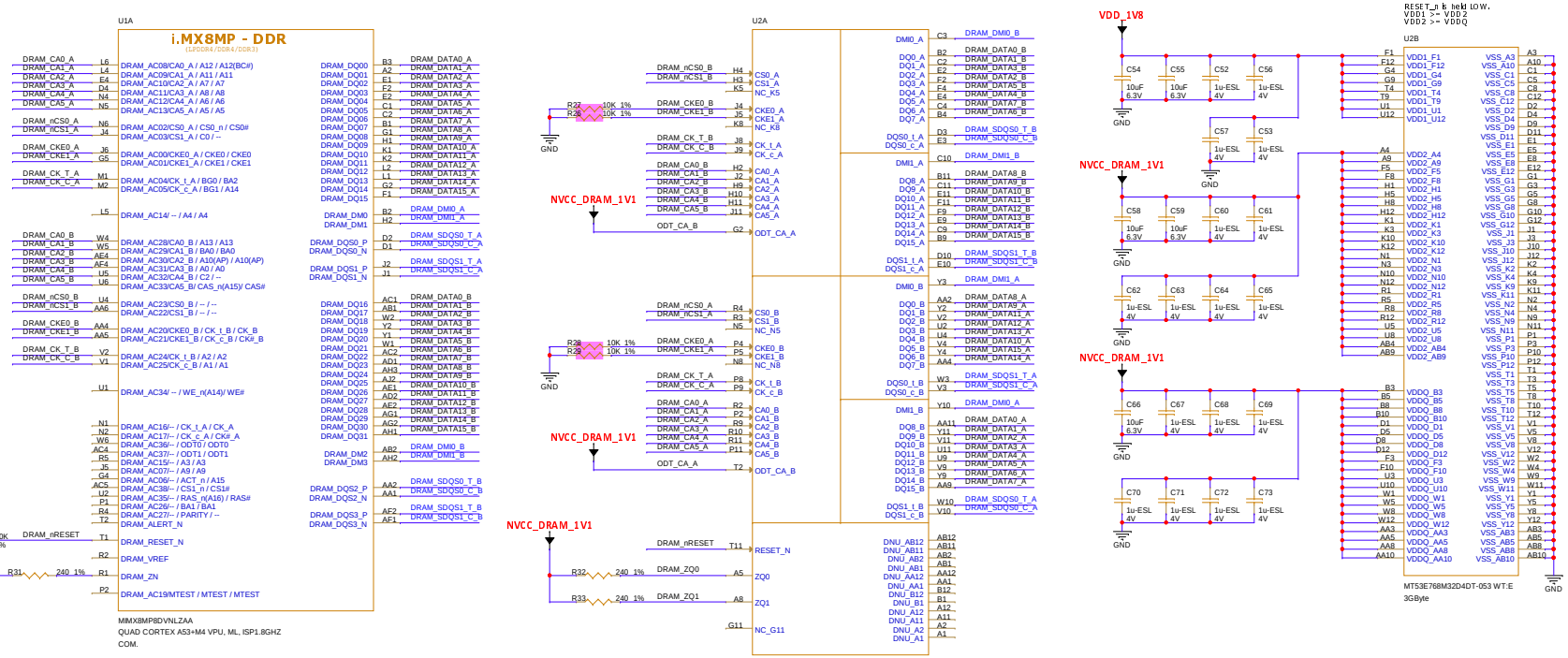


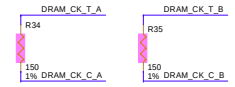
SolidRun
Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

Size	Title	Rev
C	CPU PWR	1.1

Date: Tuesday, October 03, 2023 Sheet 2 of 11

LPDDR4 6GB





Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQS_t_A
DRAM_DQS0_N	DQS0_c_A	DQS_c_A
DRAM_DM0	DMI_t_A	DMI_t_A / DBI_n_A
DRAM_DQ00	DQ0_A	DQ0_A
DRAM_DQ01	DQ1_A	DQ1_A
DRAM_DQ02	DQ2_A	DQ2_A
DRAM_DQ03	DQ3_A	DQ3_A
DRAM_DQ04	DQ4_A	DQ4_A
DRAM_DQ05	DQ5_A	DQ5_A
DRAM_DQ06	DQ6_A	DQ6_A
DRAM_DQ07	DQ7_A	DQ7_A
DRAM_DQS1_P	DQS1_t_A	DQS1_t_A
DRAM_DQS1_N	DQS1_c_A	DQS1_c_A
DRAM_DM1	DMI_t_A	DMI_t_A / DBI_n_A
DRAM_DQ08	DQ8_A	DQ8_A
DRAM_DQ09	DQ9_A	DQ9_A
DRAM_DQ10	DQ10_A	DQ10_A
DRAM_DQ11	DQ11_A	DQ11_A
DRAM_DQ12	DQ12_A	DQ12_A
DRAM_DQ13	DQ13_A	DQ13_A
DRAM_DQ14	DQ14_A	DQ14_A
DRAM_DQ15	DQ15_A	DQ15_A
DRAM_DQS2_P	DQS2_t_A	DQS_t_B
DRAM_DQS2_N	DQS2_c_A	DQS_c_B
DRAM_DQS3_P	DQS3_t_A	DQS1_t_B
DRAM_DQS3_N	DQS3_c_A	DQS1_c_B
DRAM_DM2	DMI_t_B	DMU_t_A / DBIU_n_A
DRAM_DQ16	DQ0_B	DQU0_A
DRAM_DQ17	DQ1_B	DQU1_A
DRAM_DQ18	DQ2_B	DQU2_A
DRAM_DQ19	DQ3_B	DQU3_A
DRAM_DQ20	DQ4_B	DQU4_A
DRAM_DQ21	DQ5_B	DQU5_A
DRAM_DQ22	DQ6_B	DQU6_A
DRAM_DQ23	DQ7_B	DQU7_A
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI_t_B	DMU_t_B / DBIU_n_B
DRAM_DQ24	DQ0_B	DQU0_B
DRAM_DQ25	DQ1_B	DQU1_B
DRAM_DQ26	DQ2_B	DQU2_B
DRAM_DQ27	DQ3_B	DQU3_B
DRAM_DQ28	DQ4_B	DQU4_B
DRAM_DQ29	DQ5_B	DQU5_B
DRAM_DQ30	DQ6_B	DQU6_B
DRAM_DQ31	DQ7_B	DQU7_B

Command/Address

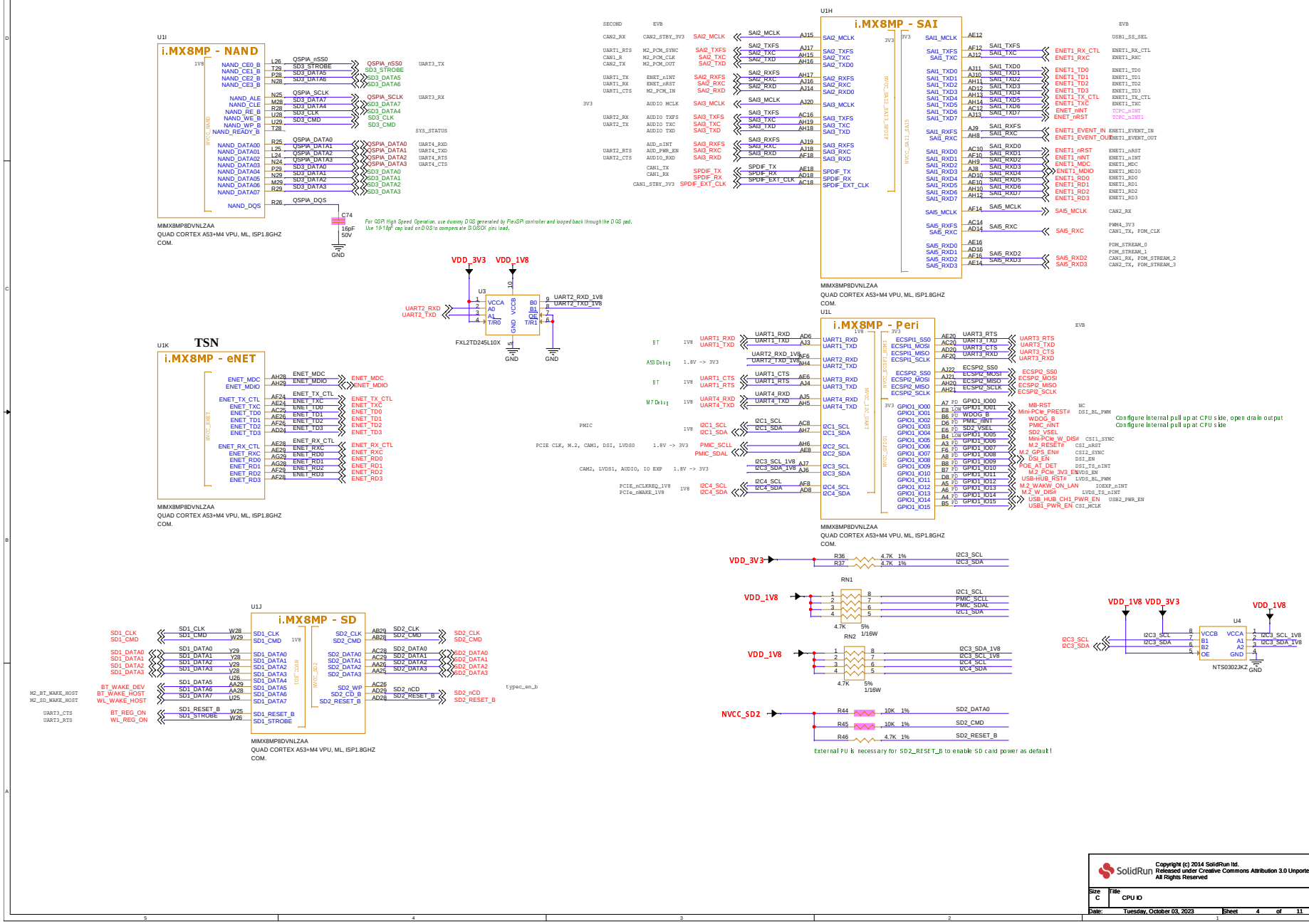
Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST	ALERT_n / MTEST
DRAM_ACD0	CKE0_A	CKE0
DRAM_ACD1	CKE1_A	CKE1
DRAM_ACD2	CS0_A	CS0_n
DRAM_ACD3	CS1_A	C0
DRAM_ACD4	CK_t_A	BG0
DRAM_ACD5	CK_c_A	BG1
DRAM_ACD6	/	ACT_n
DRAM_ACD7	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14	/	A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS1_B	/
DRAM_AC23	CS0_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34	/	WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

SolidRun
Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

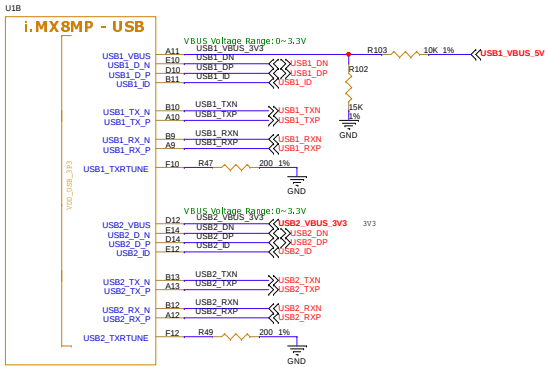
Size	Title	Rev
C	LPDDR4	1.1

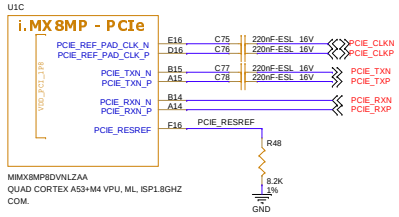
Date: Tuesday, October 03, 2023 Sheet 3 of 11

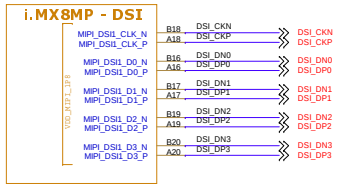
i.MX8M Plus IO Interface

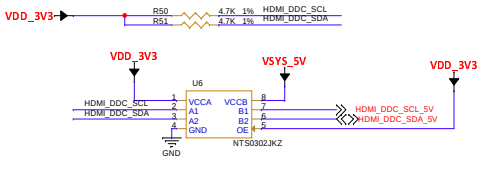


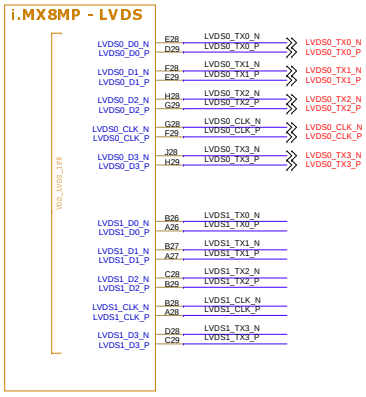
i.MX8M Plus PHYs

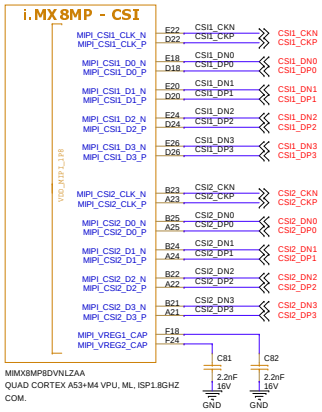


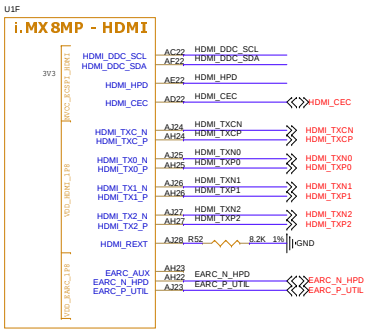










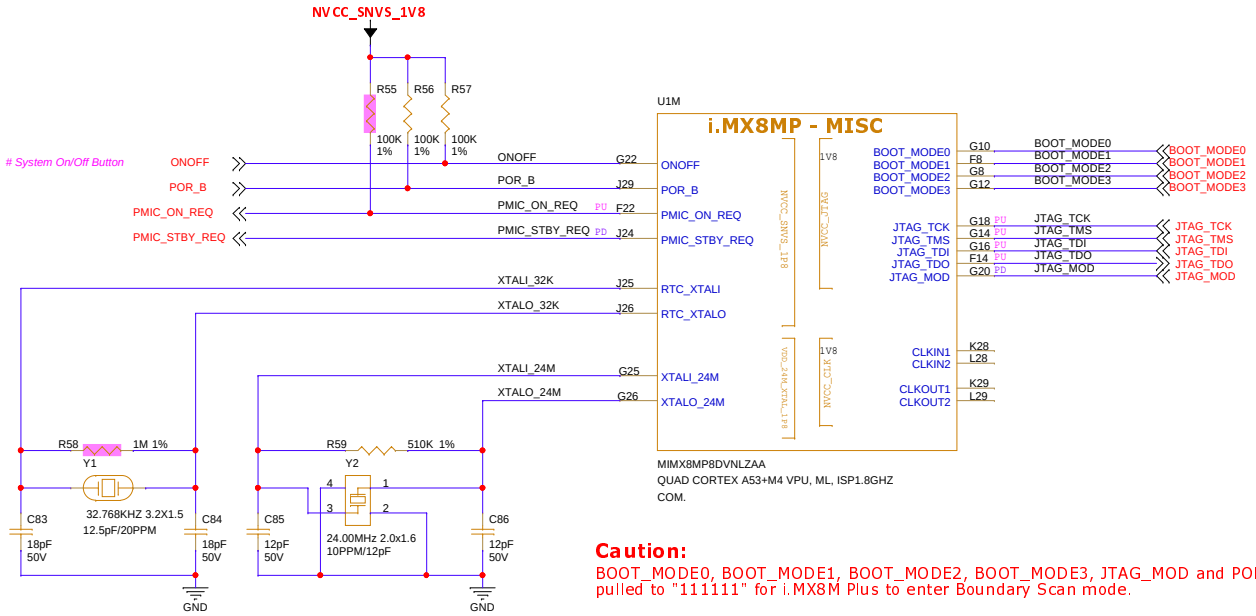


SolidRun
Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

Size	Title	Rev
C	CPU PHY	1.1

Date: Tuesday, October 03, 2023 Sheet 5 of 11

i.MX8M Plus MISC



Caution:

BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan mode.

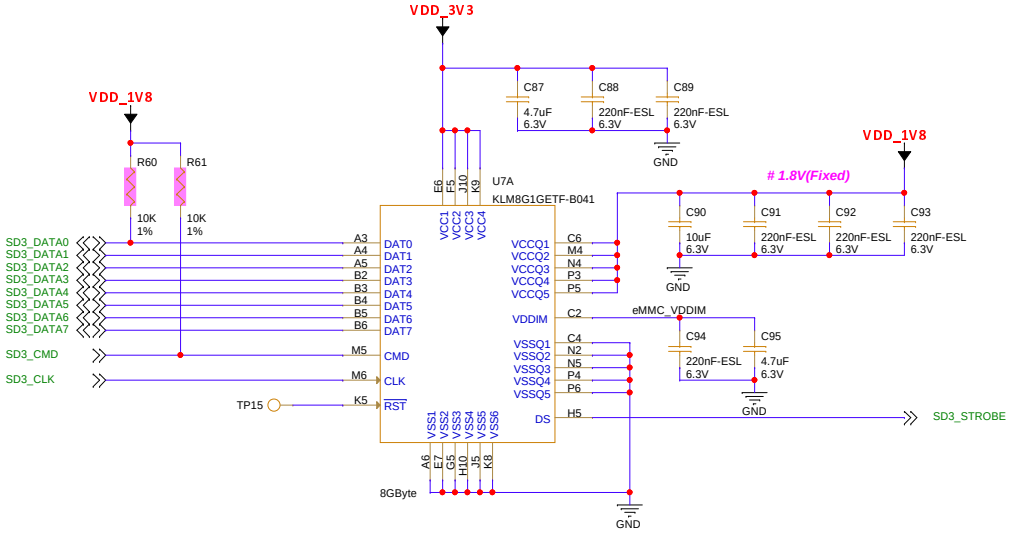
SolidRun
Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

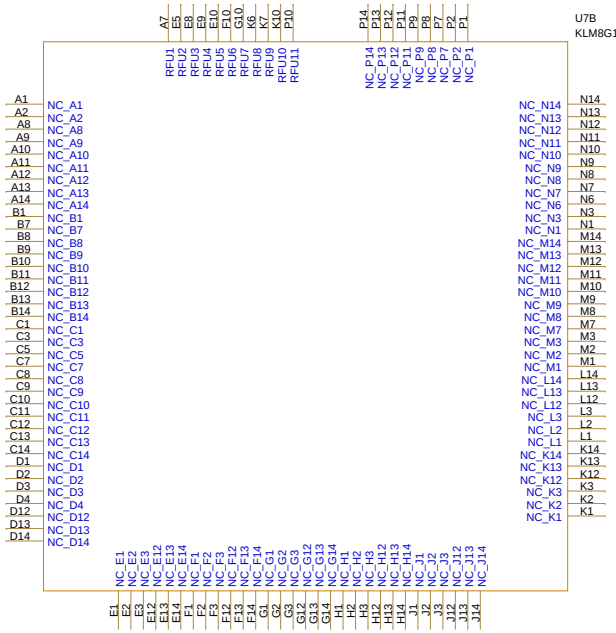
Size	Title	Rev
B	CPU MISC	1.1

Date: Tuesday, October 03, 2023 Sheet 6 of 11

Storage

eMMC5.1



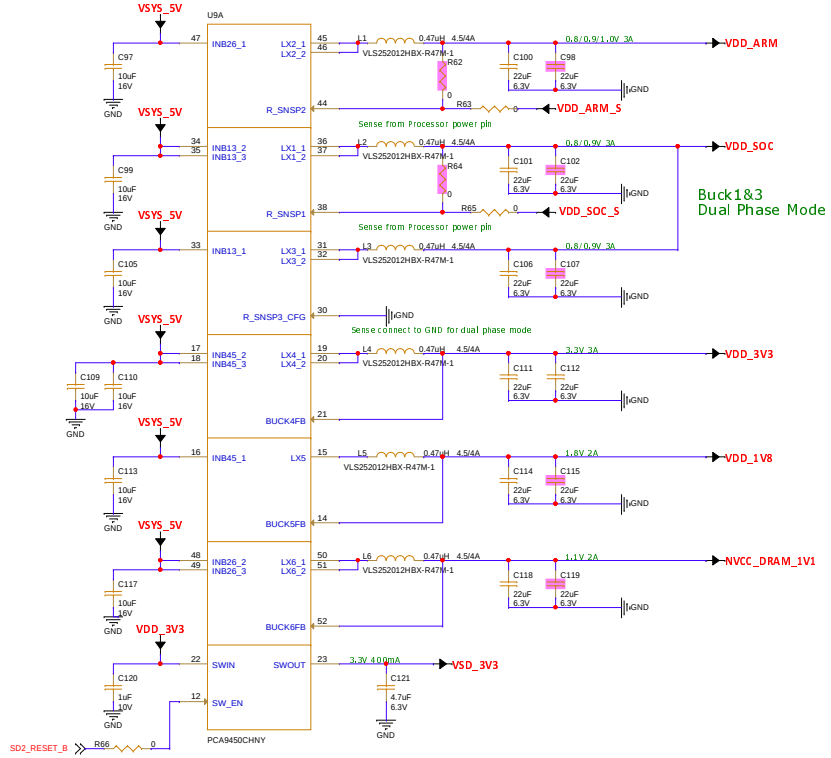


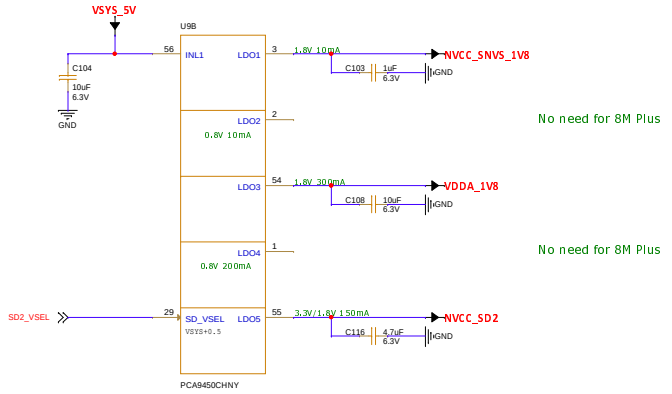
SolidRun
Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

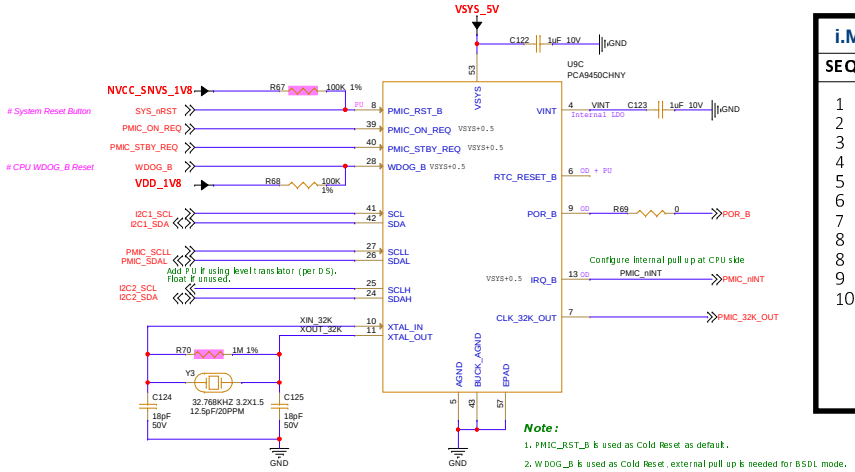
Size	Title	Rev
B	eMMC/EEPROM	1.1

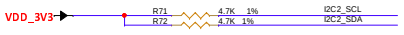
Date: Tuesday, October 03, 2023 Sheet 7 of 11

SYS PMIC









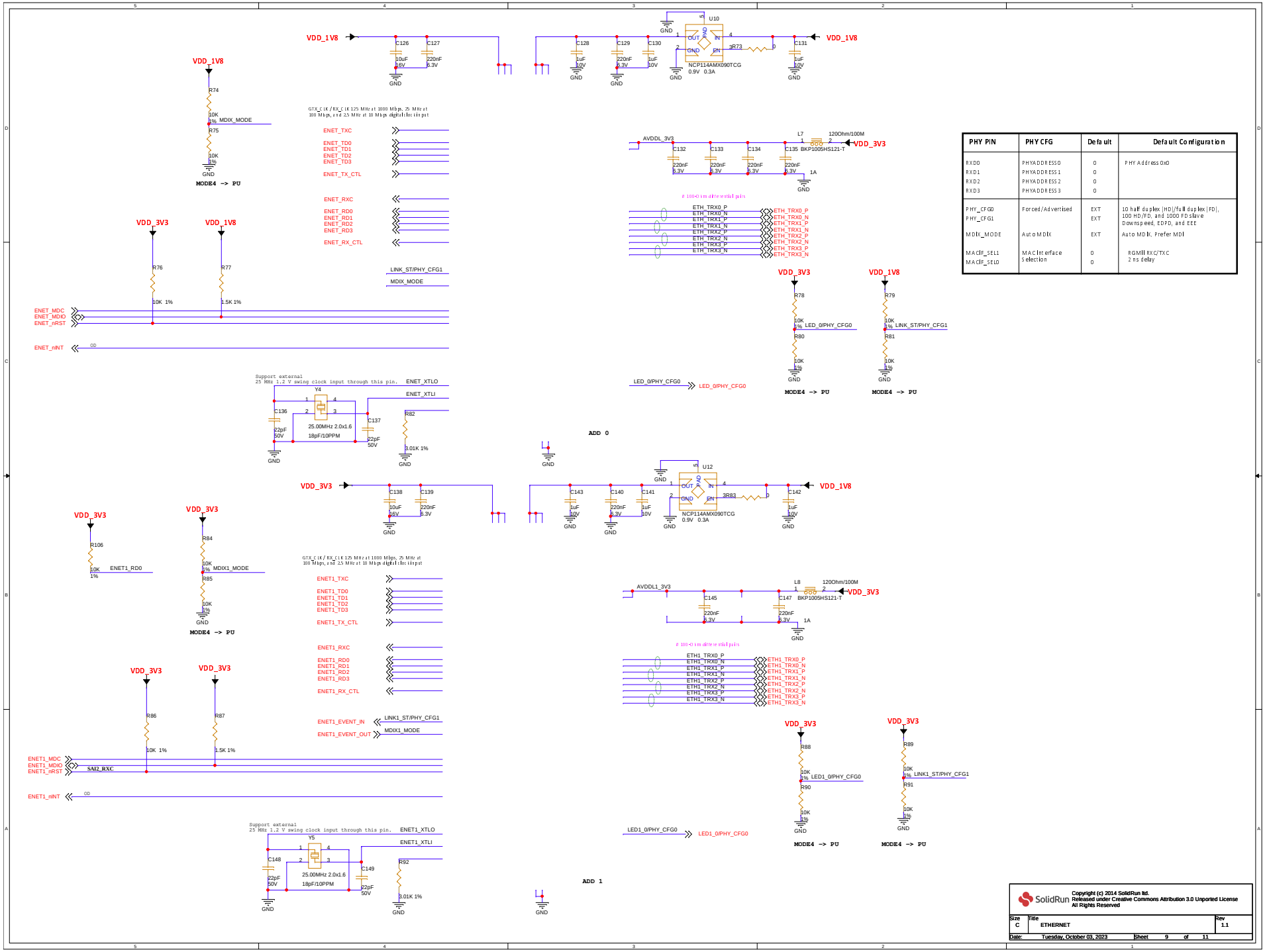
i.MX8M Plus LPDDR4 EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.65	1.8	1.95	10
2	32K_INTERNAL	RTC_CLK	--	--	--	--
3	VDD_SOC	BUCK1/3	0.72/0.81	0.85/0.95	0.9/1.0	6000
4	VDD_ARM	BUCK2	0.72/0.81/0.9	0.85/0.95/1.0	0.9/1.0/1.025	3000
5	VDDA_1V8	LDO3	1.71	1.8	1.89	300
6	VDD_1V8/NVCC_xxx	BUCK5	1.65	1.8	1.95	2000
7	NVCC_DRAM_1V1	BUCK6	1.045	1.1	1.155	2000
8	VDD_3V3/NVCC_xxx	BUCK4	3	3.3	3.6	3000
8	VSD_3V3	MUXSW	3	3.3	3.6	400
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--

SolidRun
Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

Size	Title	Rev
C	PMIC	1.1

Date: Tuesday, October 03, 2023 Sheet 8 of 11



PHY PIN	PHY CFG	Default	Default Configuration
RXD0	PHYADDRESS0	0	PHY Address 0x0
RXD1	PHYADDRESS1	0	
RXD2	PHYADDRESS2	0	
RXD3	PHYADDRESS3	0	
PHY_CFG0	Forced/Advertised	EXT	10 half duplex (HD)/full duplex (FD), 100 HD/FD, and 1000 FD slave
PHY_CFG1		EXT	Downspeed, EDPD, and EEE
MDIX_MODE	Auto MDIX	EXT	Auto MDIX, Prefer MDI
MACIF_SEL1	MAC Interface Selection	0	RGMII RXC/TXC 2 ns delay
MACIF_SEL0		0	

SolidRun
Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

Size	Title	Rev
C	ETHERNET	1.1
Date: Tuesday, October 03, 2023	Sheet 9 of 11	

Rev. 1.0	Prototype Version
Rev. 1.1	1. Change J5002 print symbol 2. Change NVCC_SA1_SA5 power rail from 1.8V to 3.3V 3. Change U13 (Second GE PHY) VDDIO to 3.3V 4. Connecting the signal SAI3_RXFS (AJ19) of the CPU to J9-41. Shouls be use as PCIe)RST in the HBP.
Rev. 1.2	1. U3 become obsolete - replaced to On-Semi 2. Change VCCA and VCCB in U4

SolidRun
Copyright (c) 2014 SolidRun ltd.
Released under Creative Commons Attribution 3.0 Unported License
All Rights Reserved

Size	Title	Rev
A	Version History	1.1

Date: Tuesday, October 03, 2023 Sheet 11 of 11