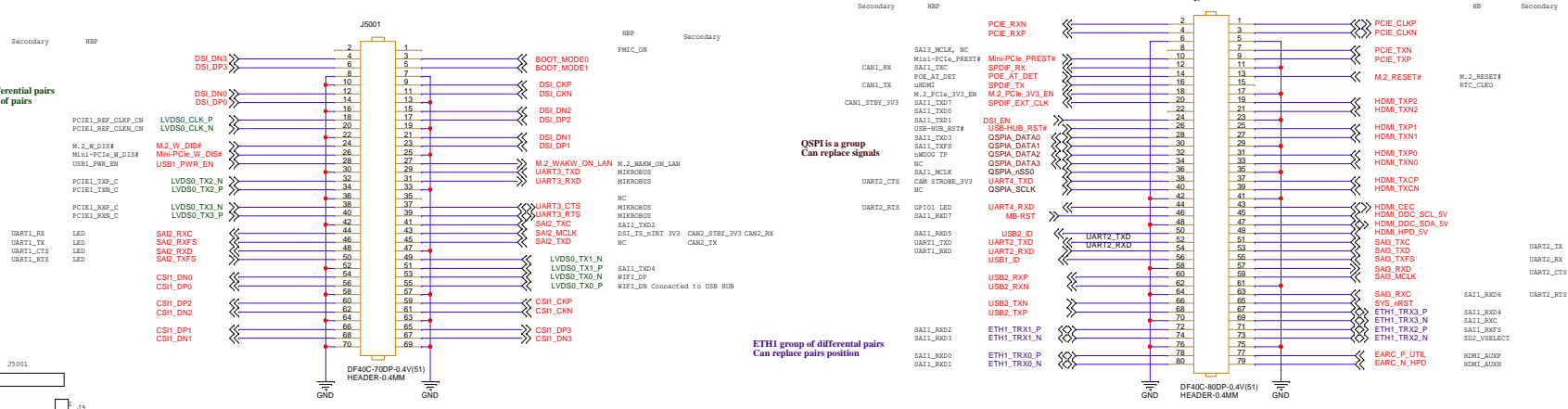
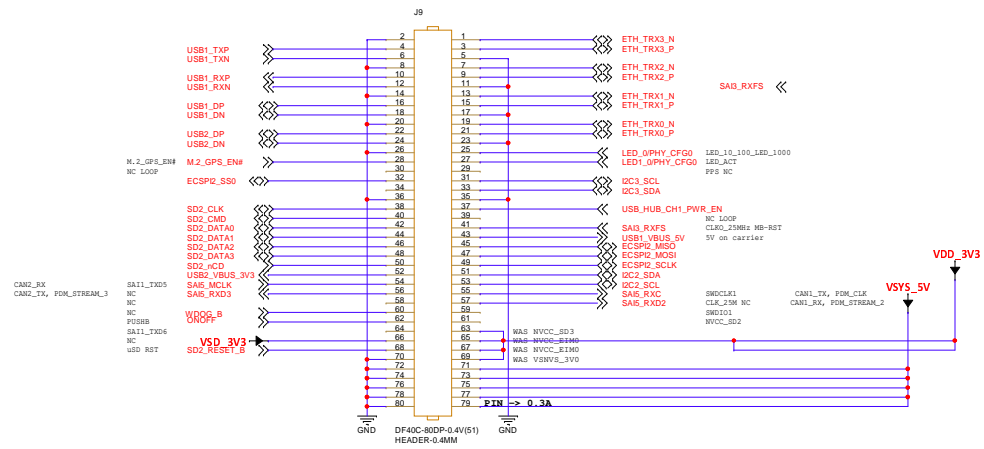


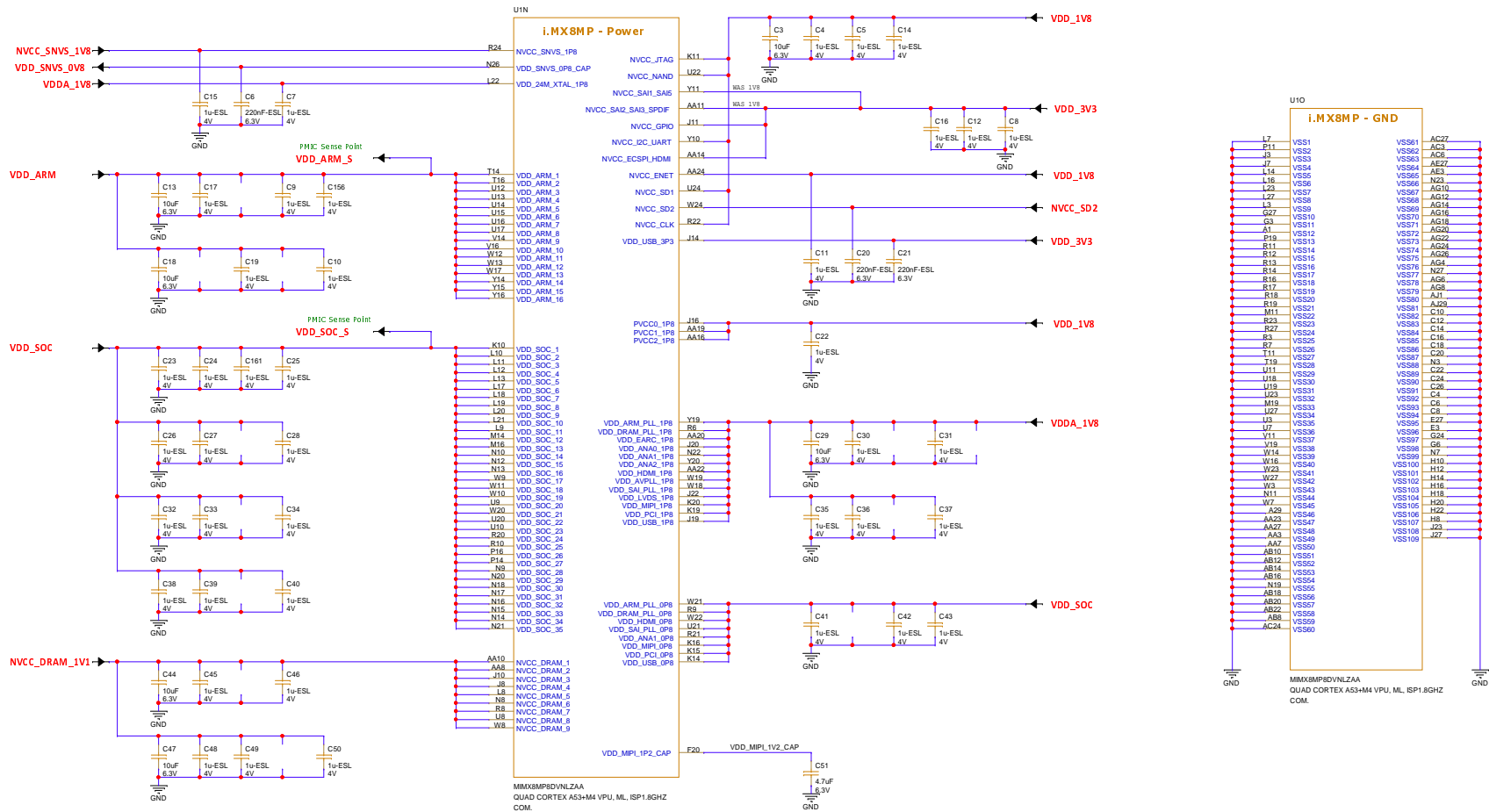
LVDS0 group of differential pairs  
Can change position of pairs



BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	Boot From Internal Fuses
0	1	USB Serial Download
1	0	USDHC3 (eMMC boot only, SD3 8-bit)
1	1	USDHC2 (SD boot only, SD2)



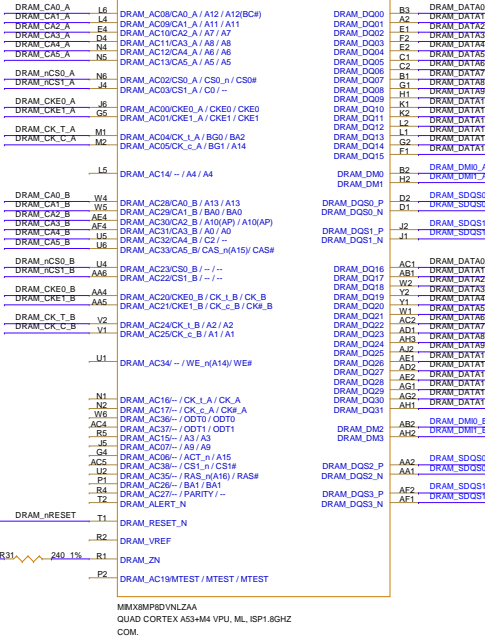
# i.MX8M Plus PWR



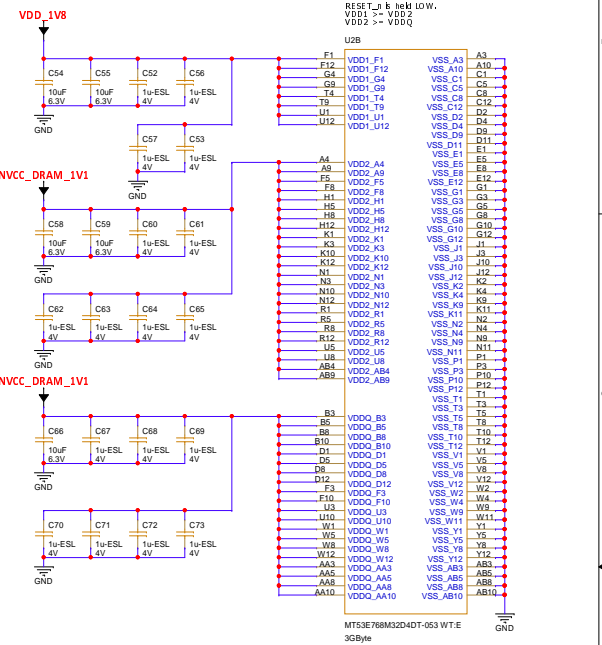
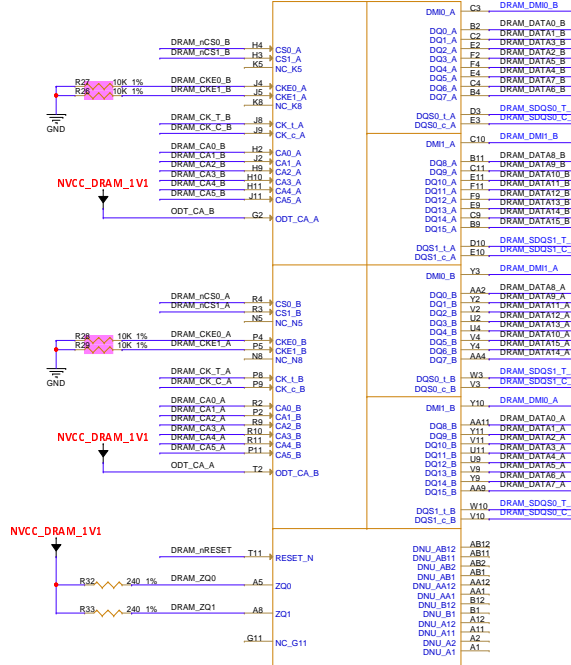
# LPDDR4 6GB

U1A

## i.MX8MP - DDR



U2A

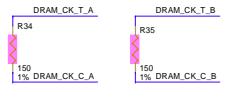


### Data Bus

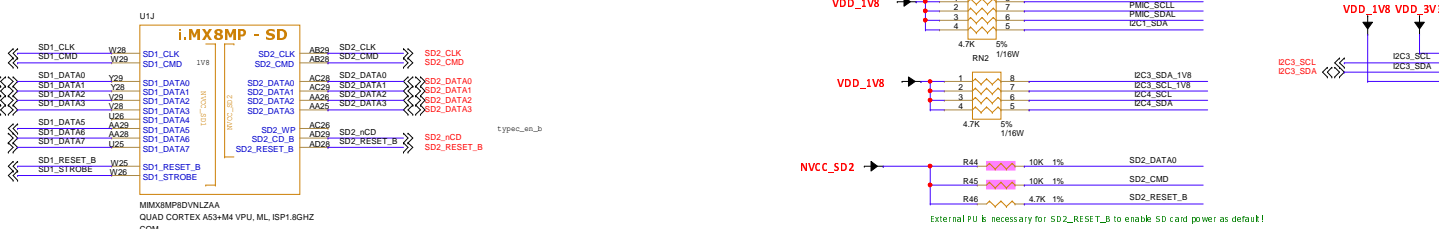
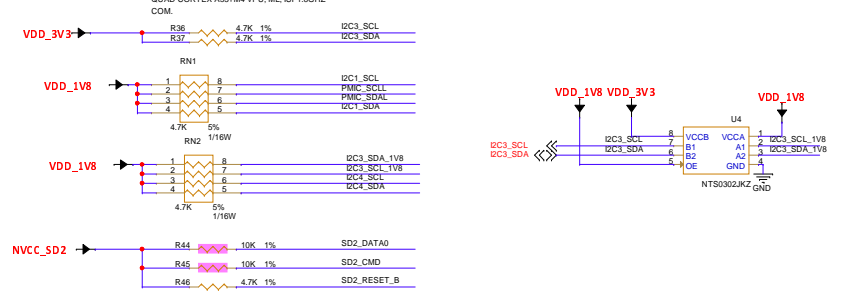
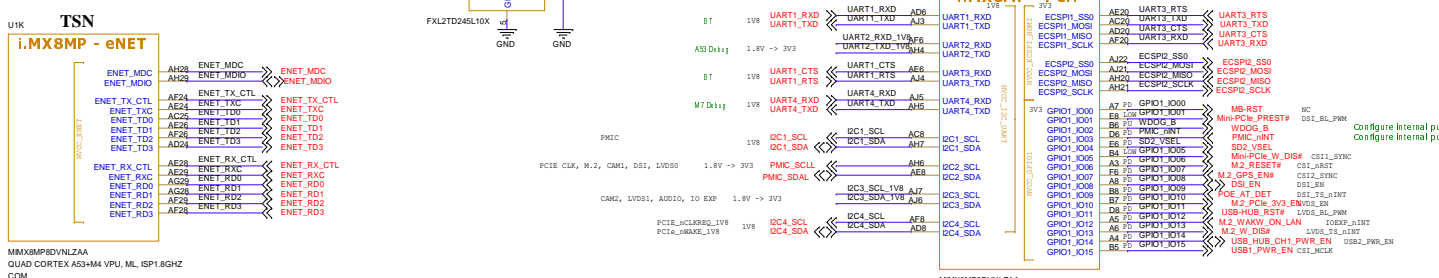
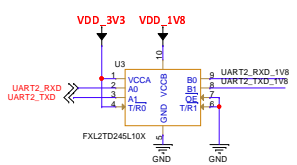
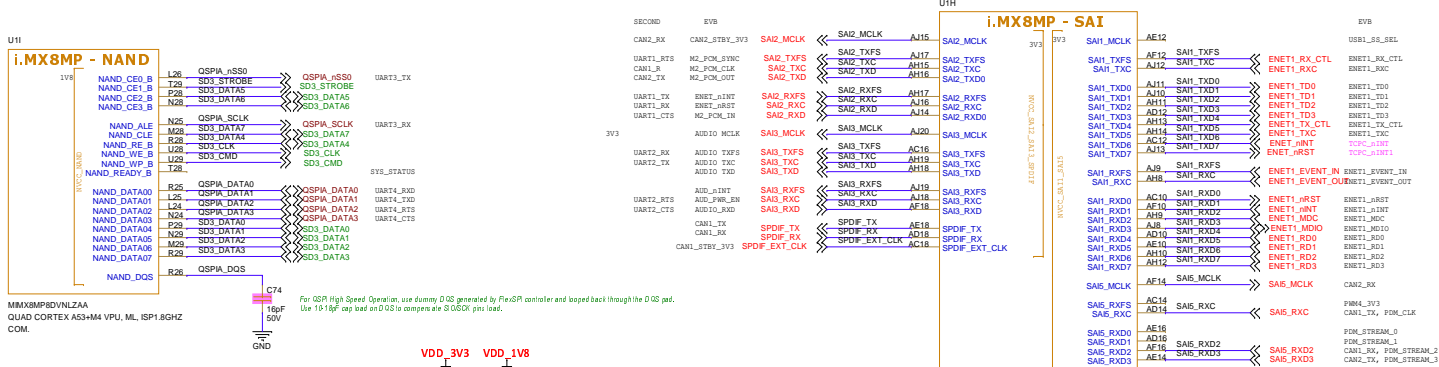
Pin Name	LPDDR4	DDR4
DRAM_D00_P	D00L_A	D00L_A
DRAM_D00_N	D00L_B	D00L_B
DRAM_D00_0	D00L_C	D00L_C
DRAM_D00_1	D00L_D	D00L_D
DRAM_D00_2	D00L_E	D00L_E
DRAM_D00_3	D00L_F	D00L_F
DRAM_D00_4	D00L_G	D00L_G
DRAM_D00_5	D00L_H	D00L_H
DRAM_D00_6	D00L_I	D00L_I
DRAM_D00_7	D00L_J	D00L_J
DRAM_D00_8	D00L_K	D00L_K
DRAM_D00_9	D00L_L	D00L_L
DRAM_D00_10	D00L_M	D00L_M
DRAM_D00_11	D00L_N	D00L_N
DRAM_D00_12	D00L_O	D00L_O
DRAM_D00_13	D00L_P	D00L_P
DRAM_D00_14	D00L_Q	D00L_Q
DRAM_D00_15	D00L_R	D00L_R
DRAM_D00_16	D00L_S	D00L_S
DRAM_D00_17	D00L_T	D00L_T
DRAM_D00_18	D00L_U	D00L_U
DRAM_D00_19	D00L_V	D00L_V
DRAM_D00_20	D00L_W	D00L_W
DRAM_D00_21	D00L_X	D00L_X
DRAM_D00_22	D00L_Y	D00L_Y
DRAM_D00_23	D00L_Z	D00L_Z
DRAM_D00_24	D00L_AA	D00L_AA
DRAM_D00_25	D00L_AB	D00L_AB
DRAM_D00_26	D00L_AC	D00L_AC
DRAM_D00_27	D00L_AD	D00L_AD
DRAM_D00_28	D00L_AE	D00L_AE
DRAM_D00_29	D00L_AF	D00L_AF
DRAM_D00_30	D00L_AG	D00L_AG
DRAM_D00_31	D00L_AH	D00L_AH

### Command/Address

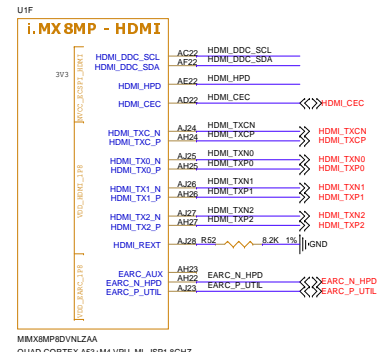
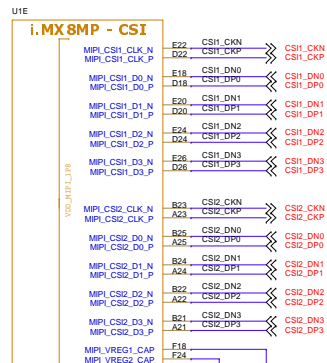
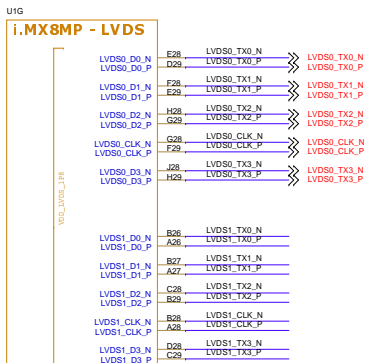
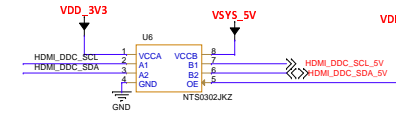
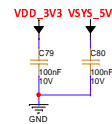
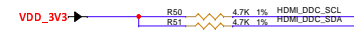
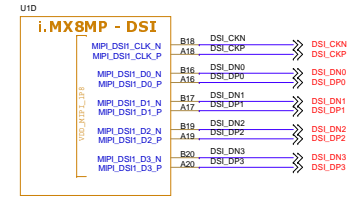
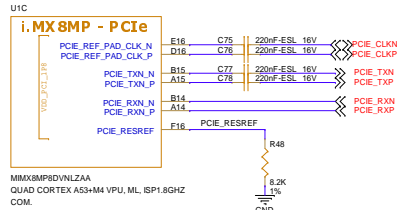
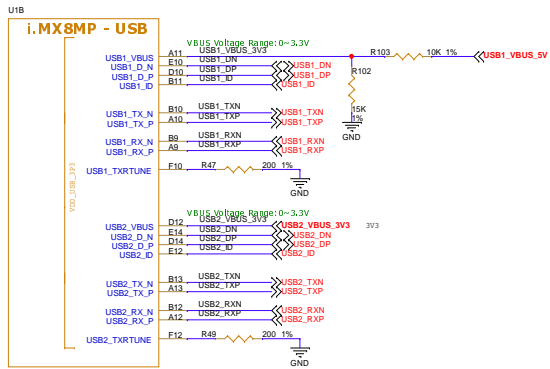
Pin Name	LPDDR4	DDR4
DRAM_RST_N	RESET_N	RESET_N
DRAM_Z00	MTEST1	RESET_N / MTEST1
DRAM_Z01	CKE0_A	CKE0_A
DRAM_Z02	CS0_A	CS0_A
DRAM_Z03	CS1_A	CS1_A
DRAM_Z04	CKLA	CKLA
DRAM_Z05	CKLB	CKLB
DRAM_Z06	CKLC	CKLC
DRAM_Z07	CKLD	CKLD
DRAM_Z08	CKLE	CKLE
DRAM_Z09	CKLF	CKLF
DRAM_Z10	CKLG	CKLG
DRAM_Z11	CKLH	CKLH
DRAM_Z12	CKLI	CKLI
DRAM_Z13	CKLJ	CKLJ
DRAM_Z14	CKLK	CKLK
DRAM_Z15	CKLM	CKLM
DRAM_Z16	CKLN	CKLN
DRAM_Z17	CKLO	CKLO
DRAM_Z18	CKLP	CKLP
DRAM_Z19	CKLQ	CKLQ
DRAM_Z20	CKLR	CKLR
DRAM_Z21	CKLS	CKLS
DRAM_Z22	CKLT	CKLT
DRAM_Z23	CKLU	CKLU
DRAM_Z24	CKLV	CKLV
DRAM_Z25	CKLW	CKLW
DRAM_Z26	CKLX	CKLX
DRAM_Z27	CKLY	CKLY
DRAM_Z28	CKLZ	CKLZ
DRAM_Z29	CKLAA	CKLAA
DRAM_Z30	CKLAB	CKLAB
DRAM_Z31	CKLAC	CKLAC
DRAM_Z32	CKLAD	CKLAD
DRAM_Z33	CKLAE	CKLAE
DRAM_Z34	CKLAF	CKLAF
DRAM_Z35	CKLAG	CKLAG
DRAM_Z36	CKLAH	CKLAH
DRAM_Z37	CKLAI	CKLAI
DRAM_Z38	CKLAJ	CKLAJ
DRAM_Z39	CKLAK	CKLAK
DRAM_Z40	CKLAL	CKLAL
DRAM_Z41	CKLAM	CKLAM
DRAM_Z42	CKLAN	CKLAN
DRAM_Z43	CKLAO	CKLAO
DRAM_Z44	CKLAP	CKLAP
DRAM_Z45	CKLAQ	CKLAQ
DRAM_Z46	CKLAR	CKLAR
DRAM_Z47	CKLAS	CKLAS
DRAM_Z48	CKLAT	CKLAT
DRAM_Z49	CKLAU	CKLAU
DRAM_Z50	CKLAV	CKLAV
DRAM_Z51	CKLAW	CKLAW
DRAM_Z52	CKLAX	CKLAX
DRAM_Z53	CKLAY	CKLAY
DRAM_Z54	CKLAZ	CKLAZ
DRAM_Z55	CKLAA	CKLAA
DRAM_Z56	CKLAB	CKLAB
DRAM_Z57	CKLAC	CKLAC
DRAM_Z58	CKLAD	CKLAD
DRAM_Z59	CKLAE	CKLAE
DRAM_Z60	CKLAF	CKLAF
DRAM_Z61	CKLAG	CKLAG
DRAM_Z62	CKLAH	CKLAH
DRAM_Z63	CKLAI	CKLAI
DRAM_Z64	CKLAJ	CKLAJ
DRAM_Z65	CKLAK	CKLAK
DRAM_Z66	CKLAL	CKLAL
DRAM_Z67	CKLAM	CKLAM
DRAM_Z68	CKLAN	CKLAN
DRAM_Z69	CKLAO	CKLAO
DRAM_Z70	CKLAP	CKLAP
DRAM_Z71	CKLAQ	CKLAQ
DRAM_Z72	CKLAR	CKLAR
DRAM_Z73	CKLAS	CKLAS
DRAM_Z74	CKLAT	CKLAT
DRAM_Z75	CKLAU	CKLAU
DRAM_Z76	CKLAV	CKLAV
DRAM_Z77	CKLAW	CKLAW
DRAM_Z78	CKLAX	CKLAX
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DRAM_Z81	CKLAA	CKLAA
DRAM_Z82	CKLAB	CKLAB
DRAM_Z83	CKLAC	CKLAC
DRAM_Z84	CKLAD	CKLAD
DRAM_Z85	CKLAE	CKLAE
DRAM_Z86	CKLAF	CKLAF
DRAM_Z87	CKLAG	CKLAG
DRAM_Z88	CKLAH	CKLAH
DRAM_Z89	CKLAI	CKLAI
DRAM_Z90	CKLAJ	CKLAJ
DRAM_Z91	CKLAK	CKLAK
DRAM_Z92	CKLAL	CKLAL
DRAM_Z93	CKLAM	CKLAM
DRAM_Z94	CKLAN	CKLAN
DRAM_Z95	CKLAO	CKLAO
DRAM_Z96	CKLAP	CKLAP
DRAM_Z97	CKLAQ	CKLAQ
DRAM_Z98	CKLAR	CKLAR
DRAM_Z99	CKLAS	CKLAS
DRAM_Z100	CKLAT	CKLAT



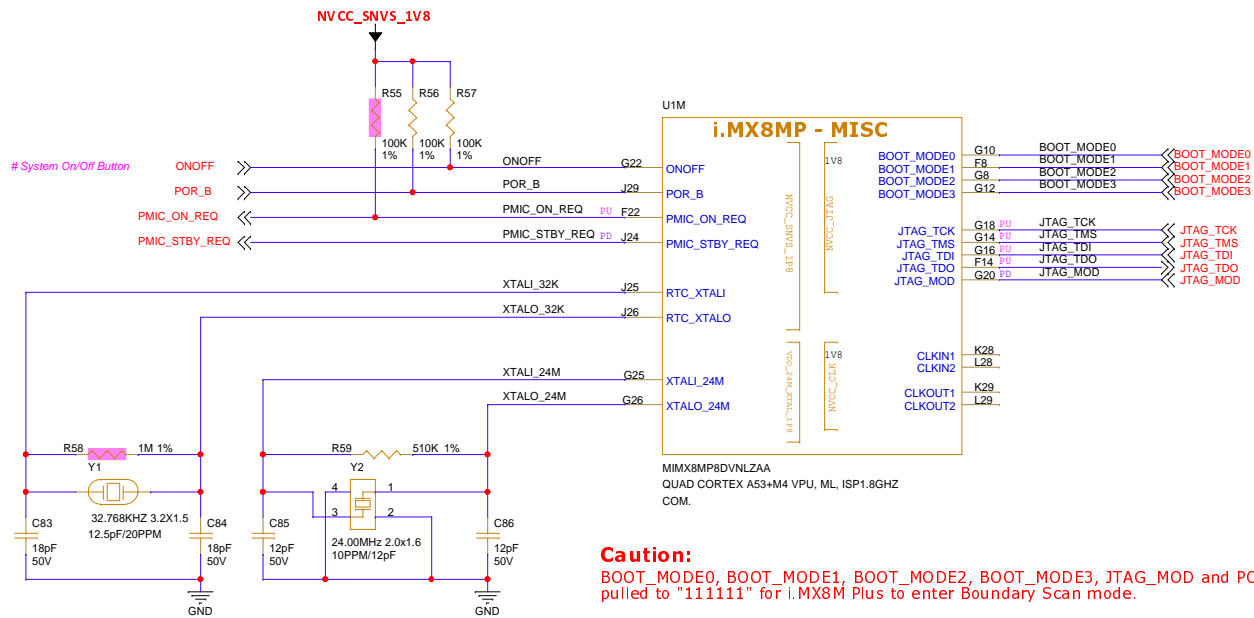
# i.MX8M Plus IO Interface



# i.MX8M Plus PHYs

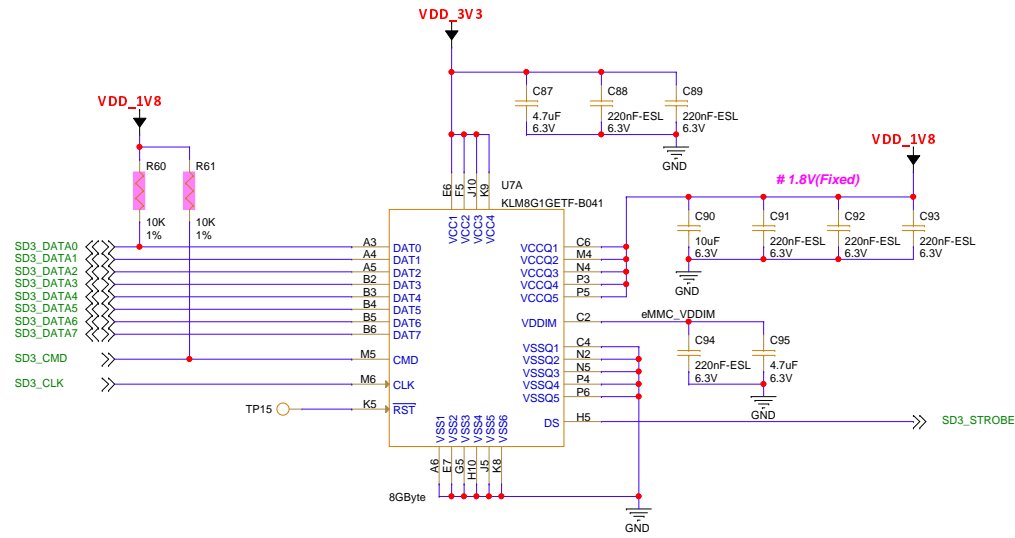


# i.MX8M Plus MISC



# Storage

## eMMC5.1

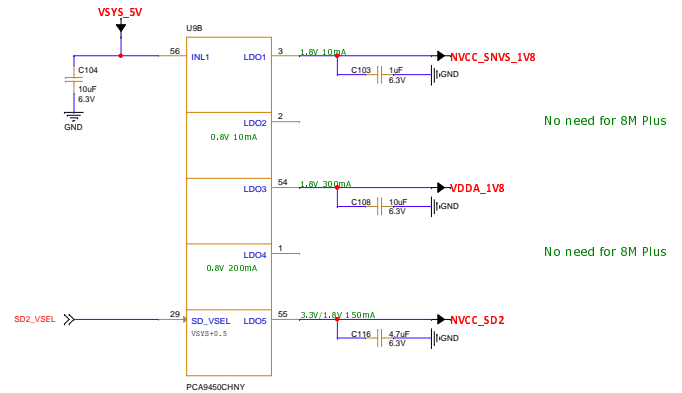
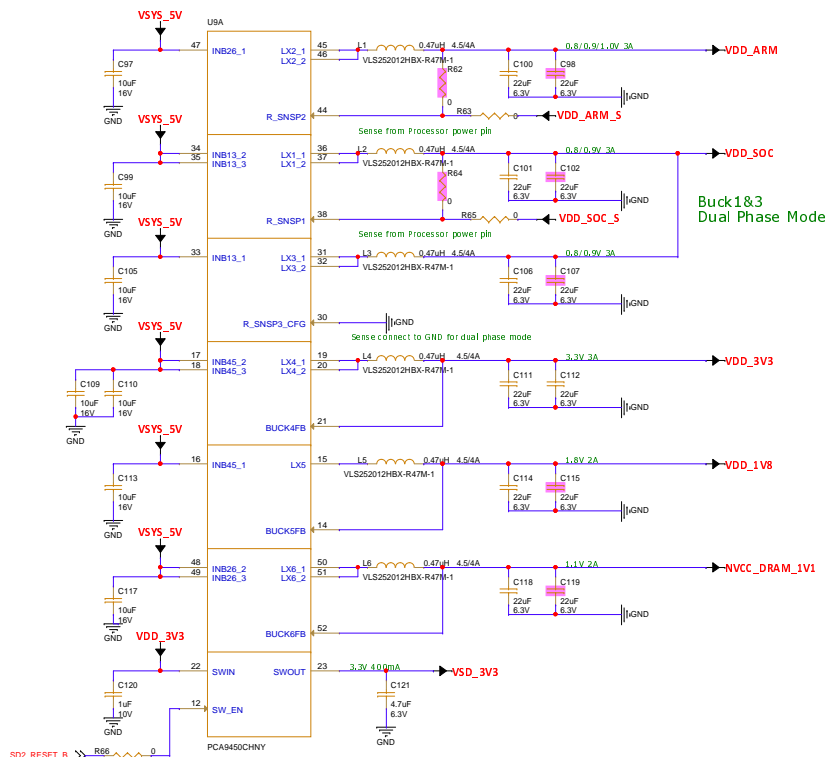


A1	NC_A1		
A2	NC_A2		
A8	NC_A8		
A9	NC_A9		
A10	NC_A10		
A11	NC_A11		
A12	NC_A12		
A13	NC_A13		
A14	NC_A14		
B1	NC_B1		
B7	NC_B7		
B8	NC_B8		
B9	NC_B9		
B10	NC_B10		
B11	NC_B11		
B12	NC_B12		
B13	NC_B13		
B14	NC_B14		
C1	NC_C1		
C3	NC_C3		
C5	NC_C5		
C7	NC_C7		
C8	NC_C8		
C9	NC_C9		
C10	NC_C10		
C11	NC_C11		
C12	NC_C12		
C13	NC_C13		
C14	NC_C14		
D1	NC_D1		
D2	NC_D2		
D3	NC_D3		
D4	NC_D4		
D12	NC_D12		
D13	NC_D13		
D14	NC_D14		
E1	NC_E1		
E2	NC_E2		
E3	NC_E3		
E13	NC_E13		
E14	NC_E14		
F1	NC_F1		
F2	NC_F2		
F3	NC_F3		
F13	NC_F13		
F14	NC_F14		
G3	NC_G3		
G3	NC_G3		
G12	NC_G12		
G13	NC_G13		
H1	NC_H1		
H2	NC_H2		
H3	NC_H3		
H13	NC_H13		
H14	NC_H14		
J1	NC_J1		
J3	NC_J3		
J12	NC_J12		
J13	NC_J13		
J14	NC_J14		
A7	RFU1		
E5	RFU2		
E8	RFU3		
E10	RFU4		
E11	RFU5		
F10	RFU6		
G10	RFU7		
K2	RFU8		
K10	RFU9		
P10	RFU10		
P10	RFU11		
P14	NC_P14		
P12	NC_P13		
P11	NC_P11		
P3	NC_P9		
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M10	NC_M10		
M8	NC_M8		
M7	NC_M7		
M3	NC_M3		
M2	NC_M2		
M1	NC_M1		
L14	NC_L14		
L13	NC_L13		
L12	NC_L12		
L3	NC_L3		
L2	NC_L2		
L1	NC_L1		
K14	NC_K14		
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K1	NC_K1		

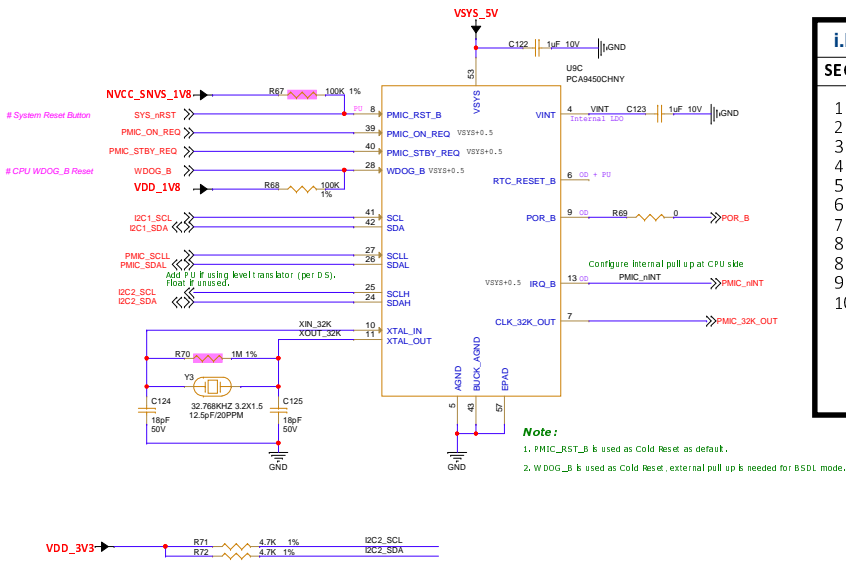
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Size	File	Rev
B	eMMC/EEPROM	1.1
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# SYS PMIC



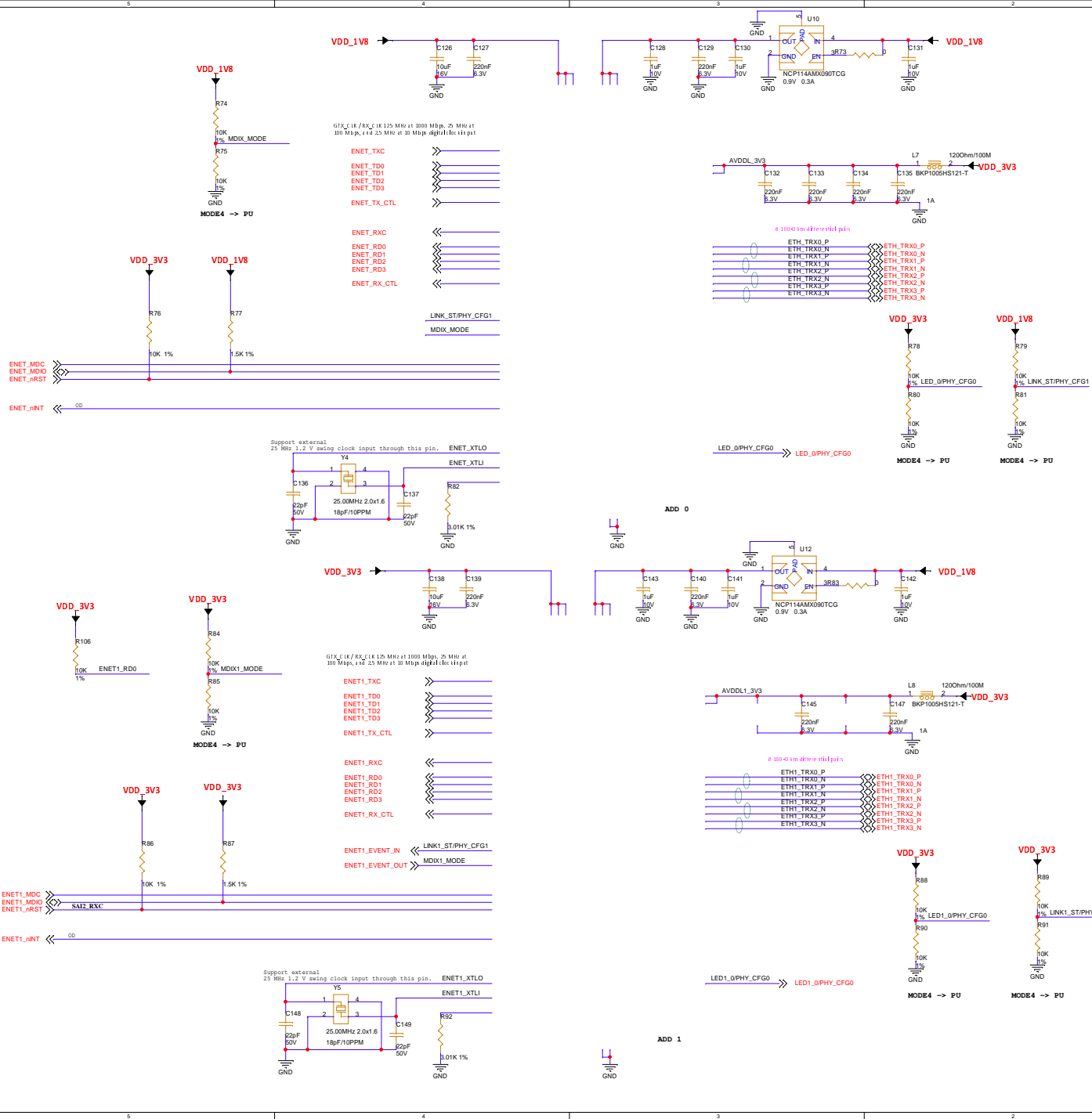
No need for 8M Plus  
No need for 8M Plus



**Note:**  
 1. PMIC\_RST\_B is used as Cold Reset as default.  
 2. WDOG\_B is used as Cold Reset, external pull up is needed for BSDL mode.

i.MX8M Plus LPDDR4 EVK Power Sequence							
SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)	
1	NVCC_SNV5_1V8	LDO1	1.65	1.8	1.95	10	
2	32K_INTERNAL	RTC_CLK	--	--	--	--	
3	VDD_SOC	BUCK1/3	0.72/0.81	0.85/0.95	0.9/1.0	6000	
4	VDD_ARM	BUCK2	0.72/0.81/0.9	0.85/0.95/1.0	0.9/1.0/1.025	3000	
5	VDDA_1V8	LDO3	1.71	1.8	1.89	300	
6	VDD_1V8/NVCC_xxx	BUCK5	1.65	1.8	1.95	2000	
7	NVCC_DRAM_1V1	BUCK6	1.045	1.1	1.155	2000	
8	VDD_3V3/NVCC_xxx	BUCK4	3	3.3	3.6	3000	
8	VSD_3V3	MUXSW	3	3.3	3.6	400	
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150	
10	POR_B	POR_B	--	--	--	--	





PHY PIN	PHY CFG	Default	Default Configuration
RXD0	PHYADDRESS0	0	PHY Address 0x0
RXD1	PHYADDRESS1	0	
RXD2	PHYADDRESS2	0	
RXD3	PHYADDRESS3	0	
PHY_CFG0	Forced/Advertised	EXT	10 half duplex (HD)/full duplex (FD), 100 HD/FD, and 1000 FD slave Downspeed, EDPD, and EEE
MDIX_MODE	Auto MDIX	EXT	Auto MDIX; Prefer MDI
MACIF_SELECT1	MAC Interface selection	0	RGMIIBU/CTIA/C
MACIF_SELECT0		0	2 ns delay

<b>Rev. 1.0</b>	Prototype Version
<b>Rev. 1.1</b>	<ol style="list-style-type: none"> <li>1. Change J5002 print symbol</li> <li>2. Change NVCC_SA1_SA5 power rail from 1.8V to 3.3V</li> <li>3. Change U13 (Second GE PHY) VDDIO to 3.3V</li> <li>4. Connecting the signal SAI3_RXFS (AJ19) of the CPU to J9-41. Should be use as PCIe)RST in the HBP.</li> </ol>
<b>Rev. 1.2</b>	<ol style="list-style-type: none"> <li>1. U3 become obsolete - replaced to On-Semi</li> <li>2. Change VCCA and VCCB in U4</li> </ol>



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Size A	Title Version History	Rev 1.1
Date:	Tuesday, October 03, 2023	Sheet 11 of 11