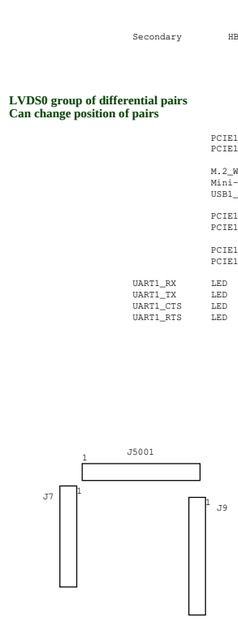

BOOT_MODE1	BOOT_MODE0	Boot Modes
0	0	Boot From Internal Fuses
0	1	USB Serial Download
1	0	USDHC3 (eMMC boot only, SD3 8-bit)
1	1	USDHC2 (SD boot only, SD2)

SRMP8QDW00D03GE008V11C0

Size	Title	Rev
C	B-T-B CONNECTORS	1.1

Date: Wednesday, February 17, 2021 Sheet 1 of 11

i.MX8M Plus PWR

U1N

i.MX8MP - Power

NVCC_SNVS_1V8 — R24 NVCC_SNVS_1P8
VDD_SNVS_0V8 — N26 VDD_SNVS_0P8_CAP
VDDA_1V8 — L22 VDD_24M_XTAL_1P8

C15 1u-ESL 4V, C6 220nF-ESL 6.3V, C7 1u-ESL 4V — GND

PMIC Sense Point
VDD_ARM_S
VDD_ARM — T14 VDD_ARM_1, T16 VDD_ARM_2, U12 VDD_ARM_3, U13 VDD_ARM_4, U14 VDD_ARM_5, U15 VDD_ARM_6, U16 VDD_ARM_7, U17 VDD_ARM_8, V14 VDD_ARM_9, V16 VDD_ARM_10, W12 VDD_ARM_11, W13 VDD_ARM_12, W17 VDD_ARM_13, Y14 VDD_ARM_14, Y15 VDD_ARM_15, Y16 VDD_ARM_16

C13 10uF 6.3V, C17 1u-ESL 4V, C9 1u-ESL 4V, C156 1u-ESL 4V — GND
C18 10uF 6.3V, C19 1u-ESL 4V, C10 1u-ESL 4V — GND

PMIC Sense Point
VDD_SOC_S
VDD_SOC — K10 VDD_SOC_1, L10 VDD_SOC_2, L11 VDD_SOC_3, L12 VDD_SOC_4, L13 VDD_SOC_5, L17 VDD_SOC_6, L18 VDD_SOC_7, L19 VDD_SOC_8, L20 VDD_SOC_9, L21 VDD_SOC_10, L9 VDD_SOC_11, M14 VDD_SOC_12, M16 VDD_SOC_13, N10 VDD_SOC_14, N12 VDD_SOC_15, N13 VDD_SOC_16, W9 VDD_SOC_17, W11 VDD_SOC_18, W10 VDD_SOC_19, U9 VDD_SOC_20, W20 VDD_SOC_21, U20 VDD_SOC_22, U10 VDD_SOC_23, R20 VDD_SOC_24, R10 VDD_SOC_25, P16 VDD_SOC_26, P14 VDD_SOC_27, N9 VDD_SOC_28, N20 VDD_SOC_29, N18 VDD_SOC_30, N17 VDD_SOC_31, N16 VDD_SOC_32, N15 VDD_SOC_33, N14 VDD_SOC_34, N21 VDD_SOC_35

C23 1u-ESL 4V, C24 1u-ESL 4V, C161 1u-ESL 4V, C25 1u-ESL 4V — GND
C26 1u-ESL 4V, C27 1u-ESL 4V, C28 1u-ESL 4V — GND
C32 1u-ESL 4V, C33 1u-ESL 4V, C34 1u-ESL 4V — GND
C38 1u-ESL 4V, C39 1u-ESL 4V, C40 1u-ESL 4V — GND

NVCC_DRAM_1V1 — AA10 NVCC_DRAM_1, AA8 NVCC_DRAM_2, J10 NVCC_DRAM_3, J8 NVCC_DRAM_4, L8 NVCC_DRAM_5, N8 NVCC_DRAM_6, R8 NVCC_DRAM_7, U8 NVCC_DRAM_8, W8 NVCC_DRAM_9

C44 10uF 6.3V, C45 1u-ESL 4V, C46 1u-ESL 4V — GND
C47 10uF 6.3V, C48 1u-ESL 4V, C49 1u-ESL 4V, C50 1u-ESL 4V — GND

NVCC_JTAG — K11
NVCC_NAND — U22
NVCC_SAI1_SAI5 — Y11 (WAS 1V8)
NVCC_SAI2_SAI3_SPDIF — AA11 (WAS 1V8)
NVCC_GPIO — J11
NVCC_I2C_UART — Y10
NVCC_ECSPI_HDMI — AA14
NVCC_ENET — AA24
NVCC_SD1 — U24
NVCC_SD2 — W24
NVCC_CLK — R22
VDD_USB_3P3 — J14

C3 10uF 6.3V, C4 1u-ESL 4V, C5 1u-ESL 4V, C14 1u-ESL 4V — GND — VDD_1V8
C16 1u-ESL 4V, C12 1u-ESL 4V, C8 1u-ESL 4V — GND — VDD_3V3
VDD_1V8
NVCC_SD2
C11 1u-ESL 4V, C20 220nF-ESL 6.3V, C21 220nF-ESL 6.3V — GND — VDD_3V3

PVCC0_1P8 — J16
PVCC1_1P8 — AA19
PVCC2_1P8 — AA16
C22 1u-ESL 4V — GND — VDD_1V8

VDD_ARM_PLL_1P8 — Y19
VDD_DRAM_PLL_1P8 — R6
VDD_EARC_1P8 — AA20
VDD_ANA0_1P8 — J20
VDD_ANA1_1P8 — N22
VDD_ANA2_1P8 — Y20
VDD_HDMI_1P8 — AA22
VDD_AVPLL_1P8 — W19
VDD_SAI_PLL_1P8 — W18
VDD_LVDS_1P8 — J22
VDD_MIPI_1P8 — K20
VDD_PCI_1P8 — K19
VDD_USB_1P8 — J19
C29 10uF 6.3V, C30 1u-ESL 4V, C31 1u-ESL 4V — GND — VDDA_1V8
C35 1u-ESL 4V, C36 1u-ESL 4V, C37 1u-ESL 4V — GND

VDD_ARM_PLL_0P8 — W21
VDD_DRAM_PLL_0P8 — R9
VDD_HDMI_0P8 — W22
VDD_SAI_PLL_0P8 — U21
VDD_ANA1_0P8 — R21
VDD_MIPI_0P8 — K16
VDD_PCI_0P8 — K15
VDD_USB_0P8 — K14
C41 1u-ESL 4V, C42 1u-ESL 4V, C43 1u-ESL 4V — GND — VDD_SOC

VDD_MIPI_1P2_CAP — F20 — VDD_MIPI_1V2_CAP
C51 4.7uF 6.3V — GND

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COM.

U1O

i.MX8MP - GND

L7 P11 J3 J7 L14 L16 L23 L27 L3 G27 G3 A1 P19 R11 R12 R13 R14 R16 R17 R18 R19 M11 R23 R27 R3 R7 T11 T19 U11 U18 U19 U23 M19 U27 U3 U7 V11 V19 W14 W16 W23 W27 W3 N11 W7 A29 AA23 AA27 AA3 AA7 AB10 AB12 AB14 AB16 N19 AB18 AB20 AB22 AB8 AC24 — VSS1 … VSS60

VSS61 AC27, VSS62 AC3, VSS63 AC6, VSS64 AE27, VSS65 AE3, VSS66 N23, VSS67 AG10, VSS68 AG12, VSS69 AG14, VSS70 AG16, VSS71 AG18, VSS72 AG20, VSS73 AG22, VSS74 AG24, VSS75 AG26, VSS76 AG4, VSS77 N27, VSS78 AG6, VSS79 AG8, VSS80 AJ1, VSS81 AJ29, VSS82 C10, VSS83 C12, VSS84 C14, VSS85 C16, VSS86 C18, VSS87 C20, VSS88 N3, VSS89 C22, VSS90 C24, VSS91 C26, VSS92 C4, VSS93 C6, VSS94 C8, VSS95 E27, VSS96 E3, VSS97 G24, VSS98 G6, VSS99 N7, VSS100 H10, VSS101 H12, VSS102 H14, VSS103 H16, VSS104 H18, VSS105 H20, VSS106 H22, VSS107 H8, VSS108 J23, VSS109 J27

GND GND

MIMX8MP8DVNLZAA
QUAD CORTEX A53+M4 VPU, ML, ISP1.8GHZ
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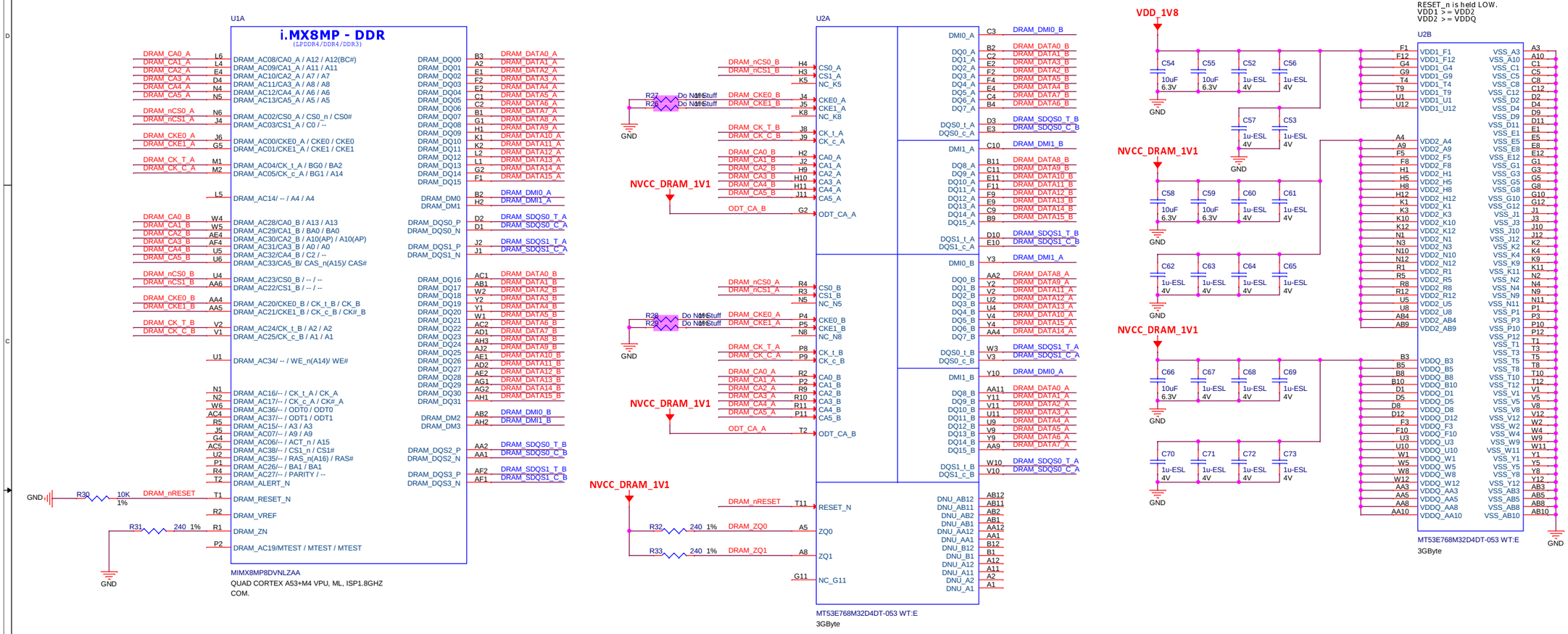
SRMP8QDW00D03GE008V11C0

Size	Title	Rev
C	CPU PWR	1.1

Date: Wednesday, February 17, 2021 Sheet 2 of 11

LPDDR4 6GB



Data Bus

Pin Name	LPDDR4	DDR4
DRAM_DQS0_P	DQS0_t_A	DQSL_t_A
DRAM_DQS0_N	DQS0_c_A	DQSL_c_A
DRAM_DM0	DMI0_A	DML_n_A / DBIL_n_A
DRAM_DQ00	DQ0_A	DQL0_A
DRAM_DQ01	DQ1_A	DQL1_A
DRAM_DQ02	DQ2_A	DQL2_A
DRAM_DQ03	DQ3_A	DQL3_A
DRAM_DQ04	DQ4_A	DQL4_A
DRAM_DQ05	DQ5_A	DQL5_A
DRAM_DQ06	DQ6_A	DQL6_A
DRAM_DQ07	DQ7_A	DQL7_A
DRAM_DQS1_P	DQS1_t_A	DQSU_t_A
DRAM_DQS1_N	DQS1_c_A	DQSU_c_A
DRAM_DM1	DMI1_A	DMU_n_A / DBIU_n_A
DRAM_DQ08	DQ08_A	DQU0_A
DRAM_DQ09	DQ09_A	DQU1_A
DRAM_DQ10	DQ10_A	DQU2_A
DRAM_DQ11	DQ11_A	DQU3_A
DRAM_DQ12	DQ12_A	DQU4_A
DRAM_DQ13	DQ13_A	DQU5_A
DRAM_DQ14	DQ14_A	DQU6_A
DRAM_DQ15	DQ15_A	DQU7_A
DRAM_DQS2_P	DQS0_t_B	DQSL_t_B
DRAM_DQS2_N	DQS0_c_B	DQSL_c_B
DRAM_DM2	DMI0_B	DML_n_B / DBIL_n_B
DRAM_DQ16	DQ0_B	DQL0_B
DRAM_DQ17	DQ1_B	DQL1_B
DRAM_DQ18	DQ2_B	DQL2_B
DRAM_DQ19	DQ3_B	DQL3_B
DRAM_DQ20	DQ4_B	DQL4_B
DRAM_DQ21	DQ5_B	DQL5_B
DRAM_DQ22	DQ6_B	DQL6_B
DRAM_DQ23	DQ7_B	DQL7_B
DRAM_DQS3_P	DQS1_t_B	DQSU_t_B
DRAM_DQS3_N	DQS1_c_B	DQSU_c_B
DRAM_DM3	DMI1_B	DMU_n_B / DBIU_n_B
DRAM_DQ24	DQ08_B	DQU0_B
DRAM_DQ25	DQ09_B	DQU1_B
DRAM_DQ26	DQ10_B	DQU2_B
DRAM_DQ27	DQ11_B	DQU3_B
DRAM_DQ28	DQ12_B	DQU4_B
DRAM_DQ29	DQ13_B	DQU5_B
DRAM_DQ30	DQ14_B	DQU6_B
DRAM_DQ31	DQ15_B	DQU7_B

Command/Address

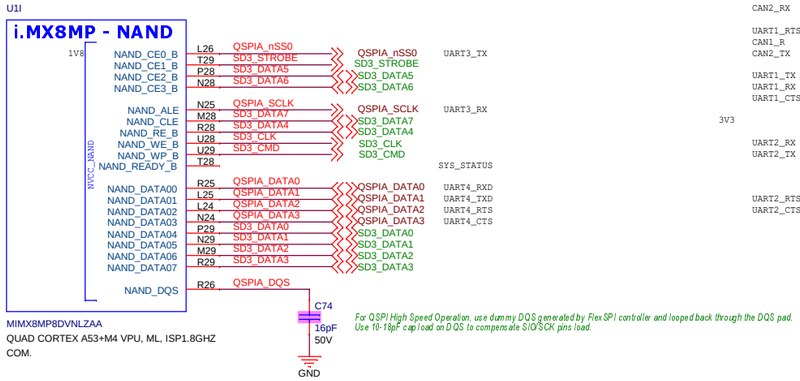
Pin Name	LPDDR4	DDR4
DRAM_RESET_N	RESET_N	RESET_n
DRAM_ALERT_N	MTEST1	ALERT_n / MTEST1
DRAM_AC00	CKE0_A	CKE0
DRAM_AC01	CKE1_A	CKE1
DRAM_AC02	CS0_A	CS0_n
DRAM_AC03	CS1_A	C0
DRAM_AC04	CK_t_A	BG0
DRAM_AC05	CK_c_A	BG1
DRAM_AC06	/	ACT_n
DRAM_AC07	/	A9
DRAM_AC08	CA0_A	A12
DRAM_AC09	CA1_A	A11
DRAM_AC10	CA2_A	A7
DRAM_AC11	CA3_A	A8
DRAM_AC12	CA4_A	A6
DRAM_AC13	CA5_A	A5
DRAM_AC14		A4
DRAM_AC15	/	A3
DRAM_AC16	/	CK_t_A
DRAM_AC17	/	CK_c_A
DRAM_AC19	MTEST	MTEST
DRAM_AC20	CKE0_B	CK_t_B
DRAM_AC21	CKE1_B	CK_c_B
DRAM_AC22	CS1_B	/
DRAM_AC23	CS0_B	/
DRAM_AC24	CK_t_B	A2
DRAM_AC25	CK_c_B	A1
DRAM_AC26	/	BA1
DRAM_AC27	/	PARITY
DRAM_AC28	CA0_B	A13
DRAM_AC29	CA1_B	BA0
DRAM_AC30	CA2_B	A10 / AP
DRAM_AC31	CA3_B	A0
DRAM_AC32	CA4_B	C2
DRAM_AC33	CA5_B	CAS_n / A15
DRAM_AC34		WE_n / A14
DRAM_AC35	/	RAS_n / A16
DRAM_AC36	/	ODT0
DRAM_AC37	/	ODT1
DRAM_AC38	/	CS1_n
DRAM_ZN	ZQ	ZQ
DRAM_VREF	VREF	VREF

SRMP8QDW00D03GE008V11C0

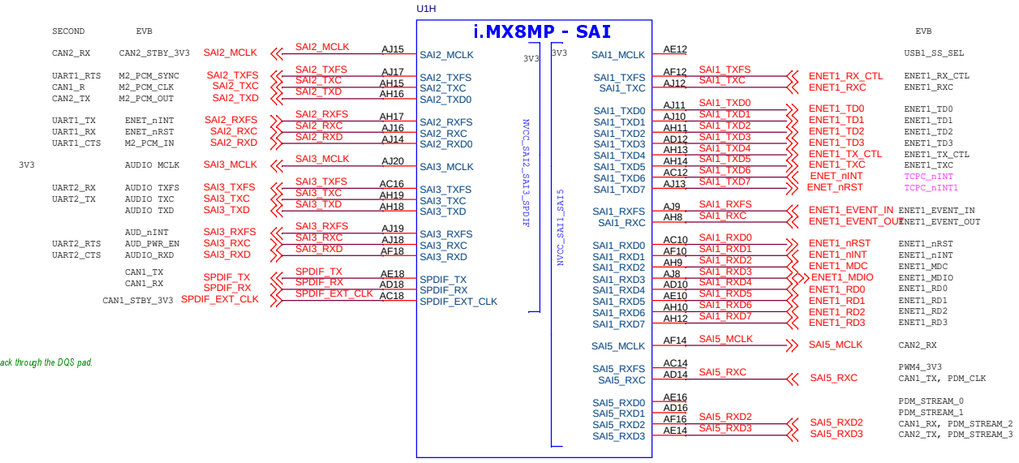
Size	Title	Rev
C	LPDDR4	1.1

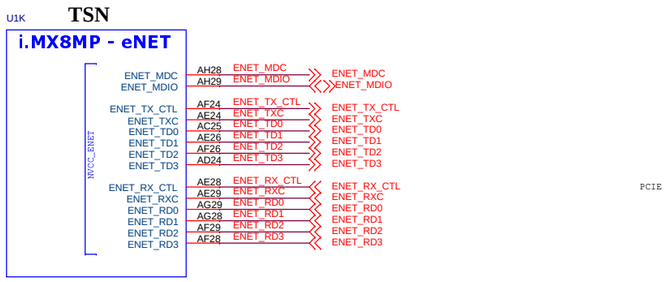
Date: Wednesday, February 17, 2021 Sheet 3 of 11

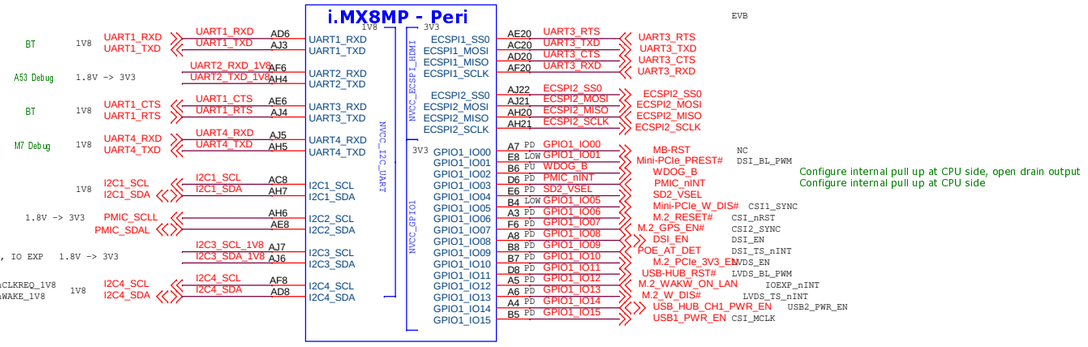
i.MX8M Plus IO Interface

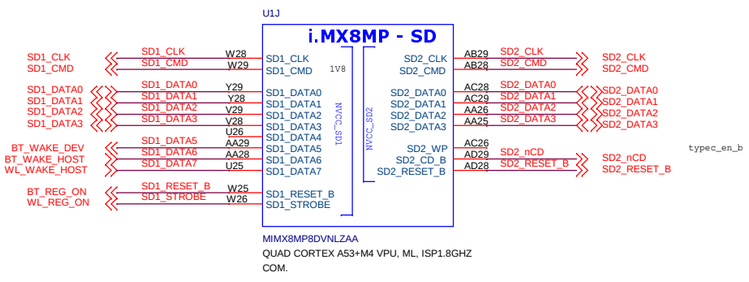


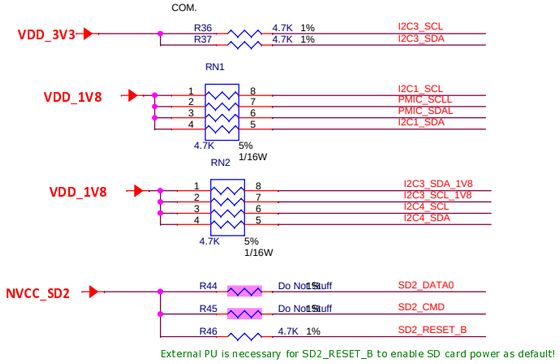
For QSPI High Speed Operation, use dummy DQS generated by FlexSPI controller and looped back through the DQS pad.
Use 10-16pF cap load on DQS to compensate SI/QSCK pins load.











External PU is necessary for SD2_RESET_B to enable SD card power as default!

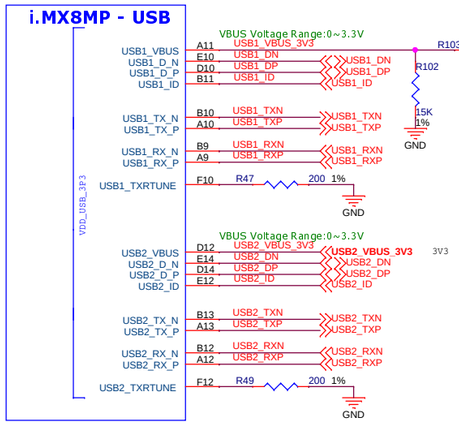
SRMP8QDW00D03GE008V11C0

Size	Title	Rev
C	CPU IO	1.1

Date: Wednesday, February 17, 2021 Sheet 4 of 11

i.MX8M Plus PHYs

U1B



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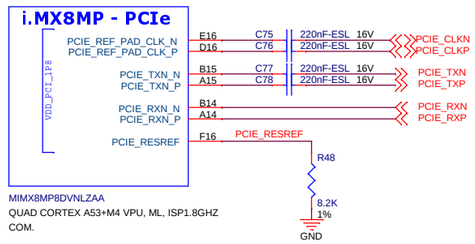
QUAD CORTEX A53+M4 VPU, ML, ISP1.8GHZ
COM.

U1C



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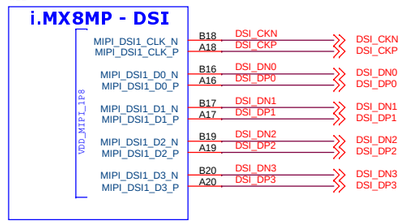
COM.

U1D



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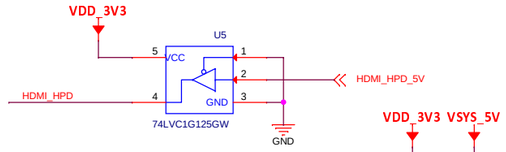
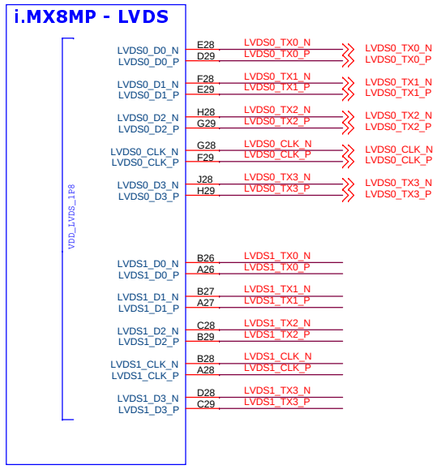


U1G



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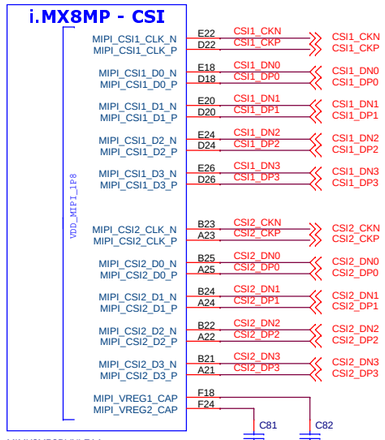
QUAD CORTEX A53+M4 VPU, ML, ISP1.8GHZ
COM.

U1E



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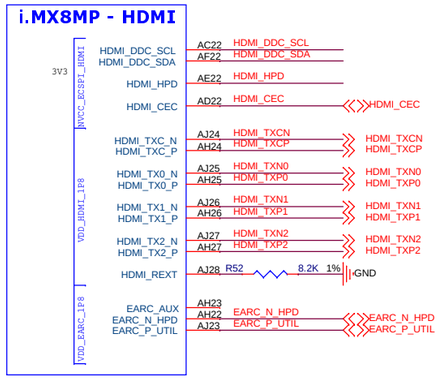
COM.

U1F



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QUAD CORTEX A53+M4 VPU, ML, ISP1.8GHZ
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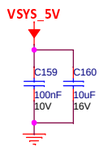
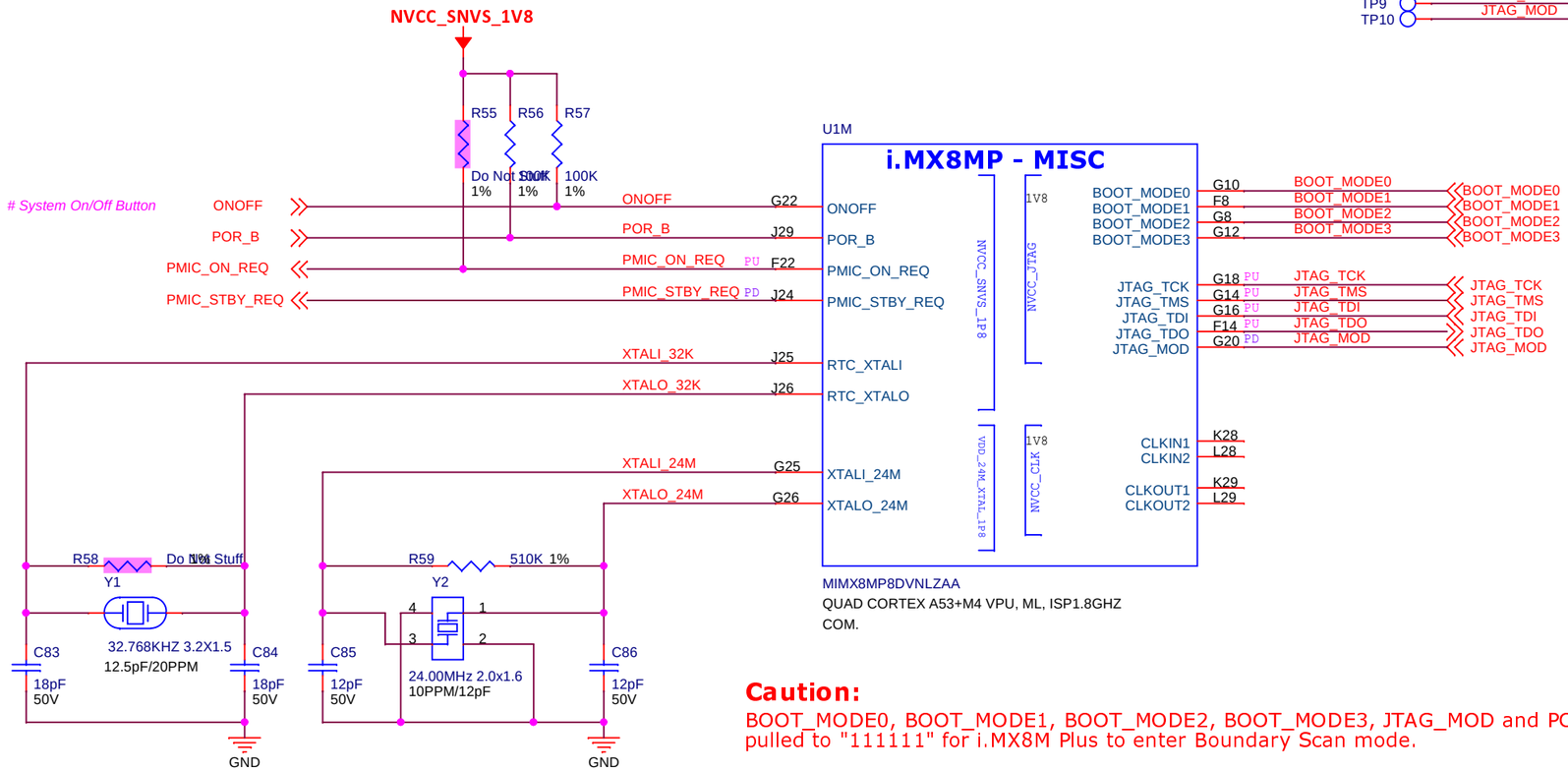


SRMP8QDW00D03GE008V11C0

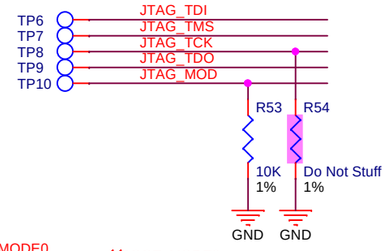
Size	Title	Rev
C	CPU PHY	1.1

Date: Wednesday, February 17, 2021 Sheet 5 of 11

i.MX8M Plus MISC



JTAG Debug



Caution:

BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan mode.

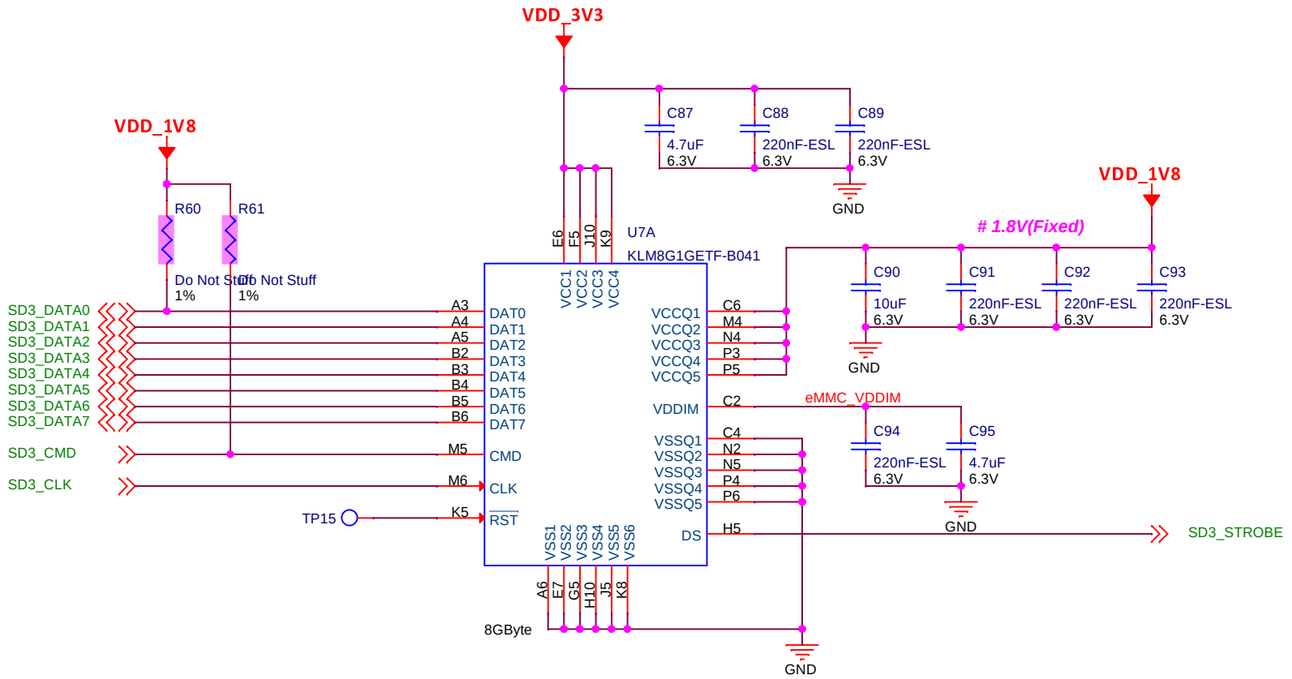
SRMP8QDW00D03GE008V11C0

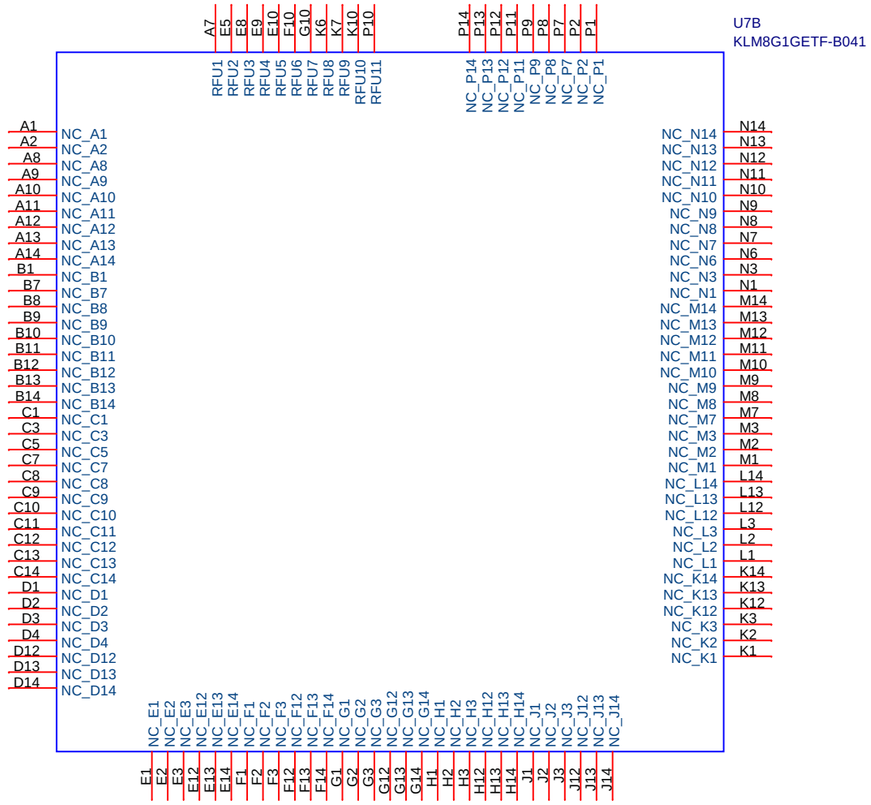
Size	Title	Rev
B	CPU MISC	1.1

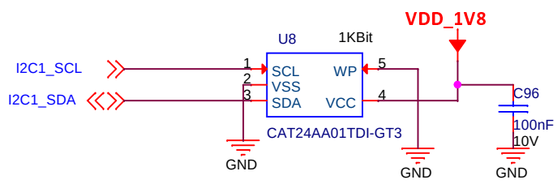
Date: Wednesday, February 17, 2021 Sheet 6 of 11

Storage

eMMC5.1





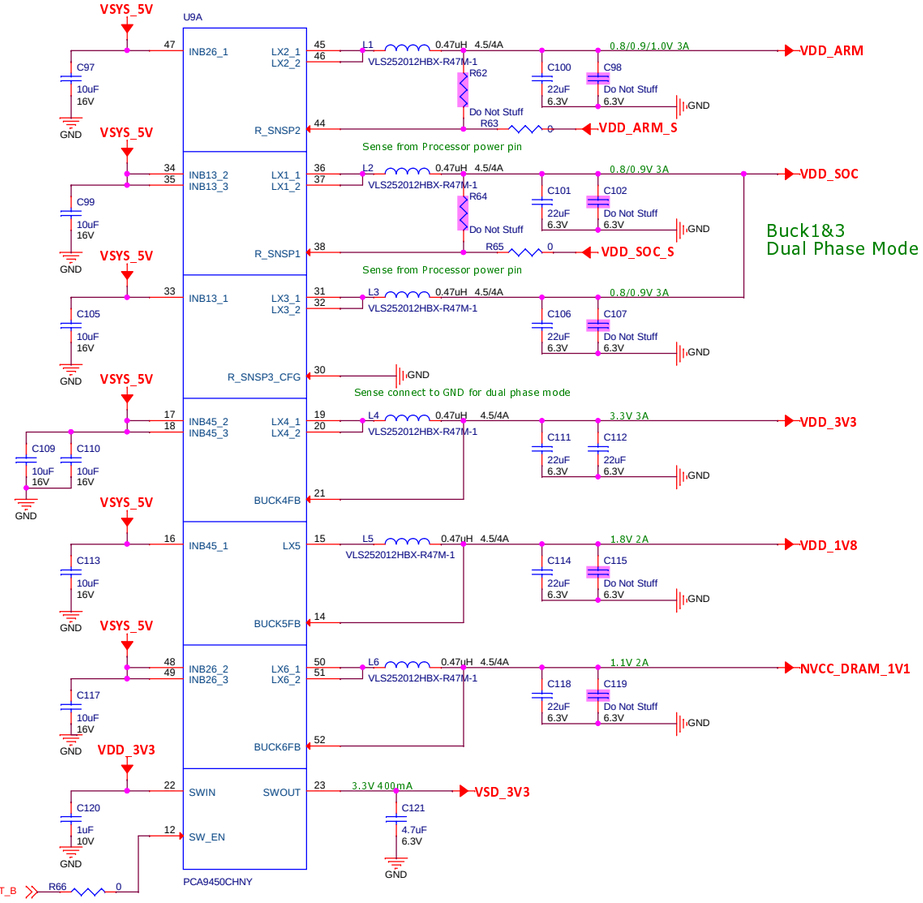


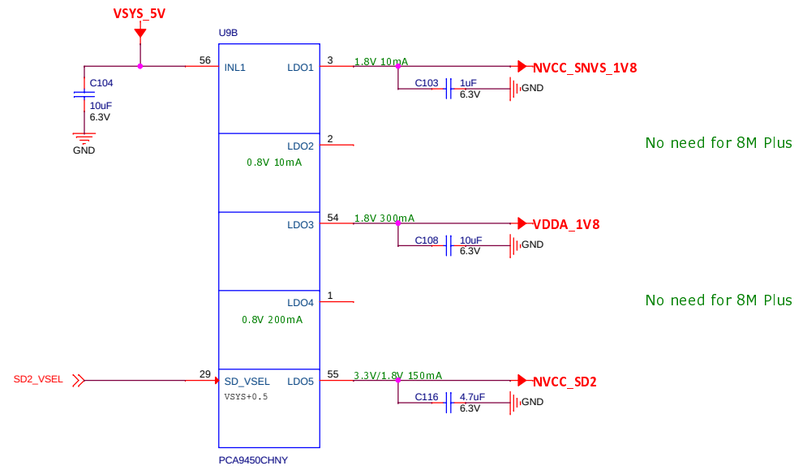
SRMP8QDW00D03GE008V11C0

Size	Title	Rev
B	eMMC/EEPROM	1.1

Date: Wednesday, February 17, 2021 Sheet 7 of 11

SYS PMIC





i.MX8M Plus LPDDR4 EVK Power Sequence

SEQ	PWR/Signal	REG	MIN	TYP	MAX	Max Current(mA)
1	NVCC_SNVS_1V8	LDO1	1.65	1.8	1.95	10
2	32K_INTERNAL	RTC_CLK	--	--	--	--
3	VDD_SOC	BUCK1/3	0.72/0.81	0.85/0.95	0.9/1.0	6000
4	VDD_ARM	BUCK2	0.72/0.81/0.9	0.85/0.95/1.0	0.9/1.0/1.025	3000
5	VDDA_1V8	LDO3	1.71	1.8	1.89	300
6	VDD_1V8/NVCC_xxx	BUCK5	1.65	1.8	1.95	2000
7	NVCC_DRAM_1V1	BUCK6	1.045	1.1	1.155	2000
8	VDD_3V3/NVCC_xxx	BUCK4	3	3.3	3.6	3000
8	VSD_3V3	MUXSW	3	3.3	3.6	400
9	NVCC_SD2	LDO5	3.0/1.65	3.3/1.8	3.6/1.95	150
10	POR_B	POR_B	--	--	--	--

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Size	Title	Rev
C	PMIC	1.1

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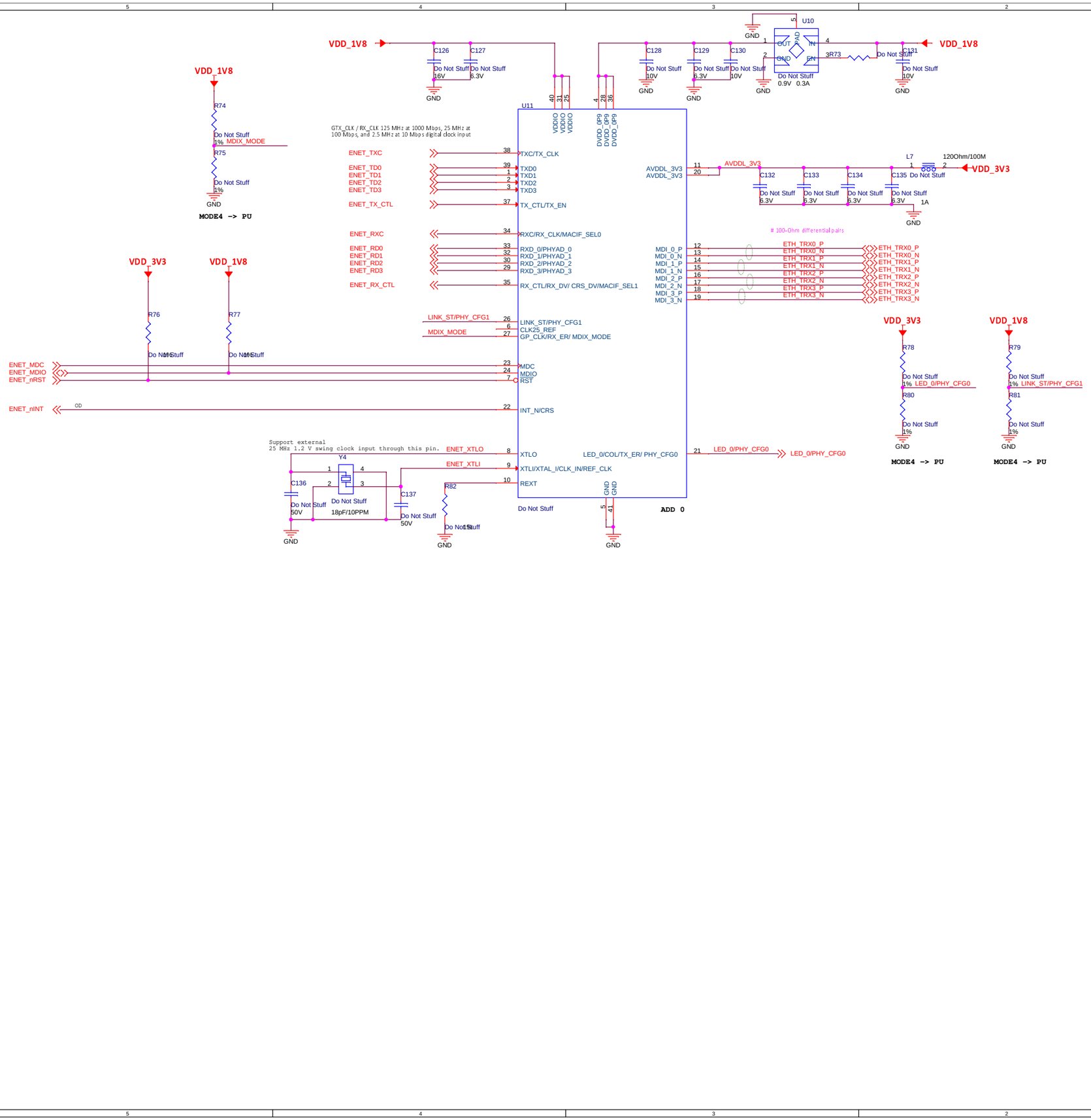

PHY PIN	PHY CFG	Default	Default Configuration
RXD0 RXD1 RXD2 RXD3	PHYADDRESS0 PHYADDRESS1 PHYADDRESS2 PHYADDRESS3	0 0 0 0	PHY Address 0x0
PHY_CFG0 PHY_CFG1	Forced/Advertised	EXT EXT	10 half duplex (HD)/full duplex (FD), 100 HD/FD, and 1000 FD slave Downspeed, EDPD, and EEE
MDIX_MODE	Auto MDIX	EXT	Auto MDIX, Prefer MDI
MACIF_SEL1 MACIF_SEL0	MAC Interface Selection	0 0	RGMII RXC/TXC 2 ns delay

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Size	Title	Rev
C	ETHERNET	1.1

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