i.MX6 SMART DEVICE SYSTEM

MCIMX6Q-SDB, MCIMX6Q-SDP, MCIMX6DL-SDP

To Extract BOM:

Item\tQuantity\tAssemblyOption\tPart\tDescription\tManufacturer\tManufacturer P\tPriorityPN\tPCB Footprint\tReference
{Item}\t{Quantity}\t{ASSY_OPT}\t{Value}\t{DESCRIPTION}\t{MFG_NAME01}\t{MFG_PN01}\t{PRIORITY_PN}\t{PCB Footprint}\t{Reference}

Assembly options naming -
1. No name - always assemble; or if DDR / processor choose one
2. DNP - Do not place
3. FE - fast ethernet
4. GE - gigabit ethernet
5. WIFI - WIFI and BT option
6. PMDDR - DDR and possibly SoC
7. PMSOC - SoC power management device
8. DDR64 - Full 64bit DDR (i.e. 4 devices)
9. PMDDR & 1.5V - 1.5 V DDR devices
10. PMDDR & 1.35V - 1.35V DDR devices

Different configuration wizard -

GENERAL DESIGN NOTES

1. Unless Otherwise Specified:
   All resistors are in ohms, 5%, 1/16 Watt
   All capacitors are in uF, 20%, 50V
   All voltages are DC
   All polarized capacitors are Tantalum

2. Critical compenents that require tolerances tighter than listed in Note 1are labeled with required tolerance on schematic. Non-critical components may be filled with tighter tolerance parts for BOM consolidation purposes, but may be changed to meet the general tolerances of Note 1 if desired.

3. Interrupted lines coded with the same letter or letter combinations are electrically connected.

4. Device type number is for reference only. The number varies with the manufacturer.

5. Special signal usage:
   _B or 'n' Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

6. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

AC ADAPTER SPECIFICATIONS

DC Voltage Output: 5VDC
Current Output: ~ 5A (depending on application)
Polarity:
Inner Diameter: 2.1mm
Outer Diameter: 5.5mm

Revision History

Rev. Code	Date	Description
X1	11/02/2011	Rev X1 Draft
A	12/15/2011	Release to Prototype Phase
AX1	02/09/12	Draft Rev B Respin: - Changed Audio CODEC to WM8962 per Marketing Request. - Removed two digital microphones. Changed mics to Wolfson WM2730 per Marketing. - Connected NVCC_JTAG rail to GEN_3V3. - Added PFET Switch to SWBST supply to isolate it from System power. - Changed HDMI Media guard to CM2020 IC to correct I2C HDMI issue. - Changed voltage sides on U9 level shifter. - Changed SW4 to 3.15V output. Moved audio 1.8V to GEN_1V8. - Changed camera 1V5 supply to VGEN6, other 1V5 loads moved to VGEN1. - Added isolation FFETs to Audio voltage supplies. - Switched USB_OTG_ID to pin ENET_RX_ER, USBOTG_OC to pin EIM2 and USBH1_OC to pin EIM_D30 to match pinmux functionality. - Added parallel termination resistors to PCIe differential clock traces. - Added next generation DEVSLP option for SATA connection. - Moved DISPO_PWR_EN to NANDF_WP_B to correct pull up voltage issue. - Deleted auxiliary 3.15V voltage regulator. - Designated several capacitors on processor core power rails as DNP. Validation proved unnecessary. - Moved I2C3_SDA from GPIO_16. This pin must be unconnected for Ethernet 1588 (time stamp) functionality to work. - Added shield ground pins to LVDS connectors. - Changed extrnal speaker capacitors to higher voltage rating. - Changed external regulator to supply 3.0V power to VSNVS. - Changed PF0100 microprocessor program circuit to DNP. - Added 5V supply to LCD expansion headers. - Connected HPOUTFB directly to Audio GND. - Connected VDDOTP to ground to boot PMIC from program settings. - Added isolation to prevent back powering board from USB when no battery present. - Back annotated Schematic to Layout. REFDES may have changed from Rev A. - Populated optional "PWRON" button circuit for use with Android. - Removed write protect on NOR Flash. - Removed LC filter circuit from external speakers. - Added an additional 2 100uF capacitors to MPCIE_3V3 next to connector. - Updated Power Rail, IOMUX, and Configuration Tables.
B	02/17/12	Release to Production
B1	04/11/12	Release to Production - Depopulated Q512 because of schematic error. - Cut trace to U12 pin 5 to prevent false USB plug in detects. - Added schematic page to detail applicable board TDAs that affect Rev B boards. - Populating CAN components U517 and U518 per Marketing Request. - Added resistor RX1 across pads for C55 to improve 24MHz clock stability. - Pull up resistors R629 and R639 have been changed to DNP.
B2	05/04/12	- Changed Marketing part number to MCIMX6Q-SDP - Changed R7, R112 and R585 to DNP - Changed C540 to "POPULATED"
B3	05/25/12	- Changed DDR3 Memory to new 1.35V capable memory MT41K128M16JT. - Changed C540 to 1.0 uF per Wolfson recommendation. - Changed R183 and R189 to 2.37K pull ups to bring I2C rise time into specification.
B4	07/18/12	- Removed buffers U500 and U520 from digital microphone data outputs. A note is added to show required hand wire modification. - The Battery Charge Done LED is disconnected and R522 is depopulated. New parts RX2, CX1 and UX1 are added. Traces show required hand modifications. - Optional Power On Circuit has been disabled and U511 and R578 are now DNP. A new Diode DX1 has been added to allow EIM_D29 to sense a button press. - RESET button SW2 now connects to the PWRON pin of the PMIC. - Added 10K pull down resistor RX3 to SDCKE0 trace. - SIM Card Connector CON1 is now populated by default. - Battery Connector Header CON3 is now populated by default. - Changed resistors R174 and R176 and to depopulated by default. LVDS0 EDID will not be connected to I2C2 channel unless needed. - Replaced digital microphones with Analog Devices ADMP421. - Disabled USB_DEF_GRN_LED circuit. Configured GPIO_1 for WDOG_B output.
B5	09/20/12	- Changed U1 to i.MX 6 T01.2 processor. - Changed C68 and C612 to DNP. - Populated C682 and C716 with 22uF capacitors.
C	09/12/12	- All hand wire changes made in Revision B4 are now formally made in the netlist and the layout files. - Q512 is changed to populated. - Optional Start Up circuit has been modified. - PMIC Programming Micro-Processor is removed. - CX1 capacitor is changed to C504 - DX1 diode is changed to D4 - RX1 resistor changed to R216 - RX2 resistor changed to R19 - RX3 resistor changed to R635 - UX1 buffer changed to U507 - Add DNP Input to U13 buffer for USB_OTG_PWR_EN. Buffer now powered from GEN_3V3. - FA_ANA and VDD_FA signals now connected to ground. - Added resistor options to EIM_DA7 trace to EPD connector. - Connected EIM_DA9 to EPDC connector JS08 to supply SDCE5 if needed. - Optional LDO U9 is now depopulated. - Added Connector J13 to support BT from SDIO Card through DNP resistors. - Added GPIO control of Battery Charge Enable pins through DNP resistor. - Changed C594 to 0.22uF - Changed C31 to 47uF. - Added C555 as second 22uF capacitor in parallel with C546. - Changed C561, C562, C586 and C596 to 0.47uF. - Added additional 47uF bulk capacitor C769 to SD2 socket VDD supply. - Added option to route HDMI DDC comms seperate from I2C2 comms channel. - C597 populated to provide de-bounce to RESET circuit. - Depopulated C68, C612. Populated C682, C716 closer to pins. - Depopulated C39, C606, C607, C608, C609, C610, C673 and C681. - Added DNP R302 to provide alternate 5V supply path to USB_H1_VBUS. - Added DNP R632 to provide alternate gating of PMIC_5V source (tied to VDDSOC). - Added DNP L25 and L26 to provide alternate 2.8V supply path to camera modules. - Added test pads to LVDS third data lanes to support testing with will 24-bit panels. - Changed capacitors C6 and C7 to Zero Ohm resistors R307 and R308 per PCIe Spec.
C1	09/27/12	- Changed Ref Des R307 and R308 back to C6 and C7 to match layout netlist.
C2	11/09/12	- Moved Ferrite Beads L10 and L17 to pads for L15 and L26. Camera Analog Voltage supply moved to VGEN3. - Added notes for 24MHz crystal and USB layout design. - Changed R17, R21, R25, R27, R68, R85, R582, and R660 to 1% resistors due to lead time availability issues.

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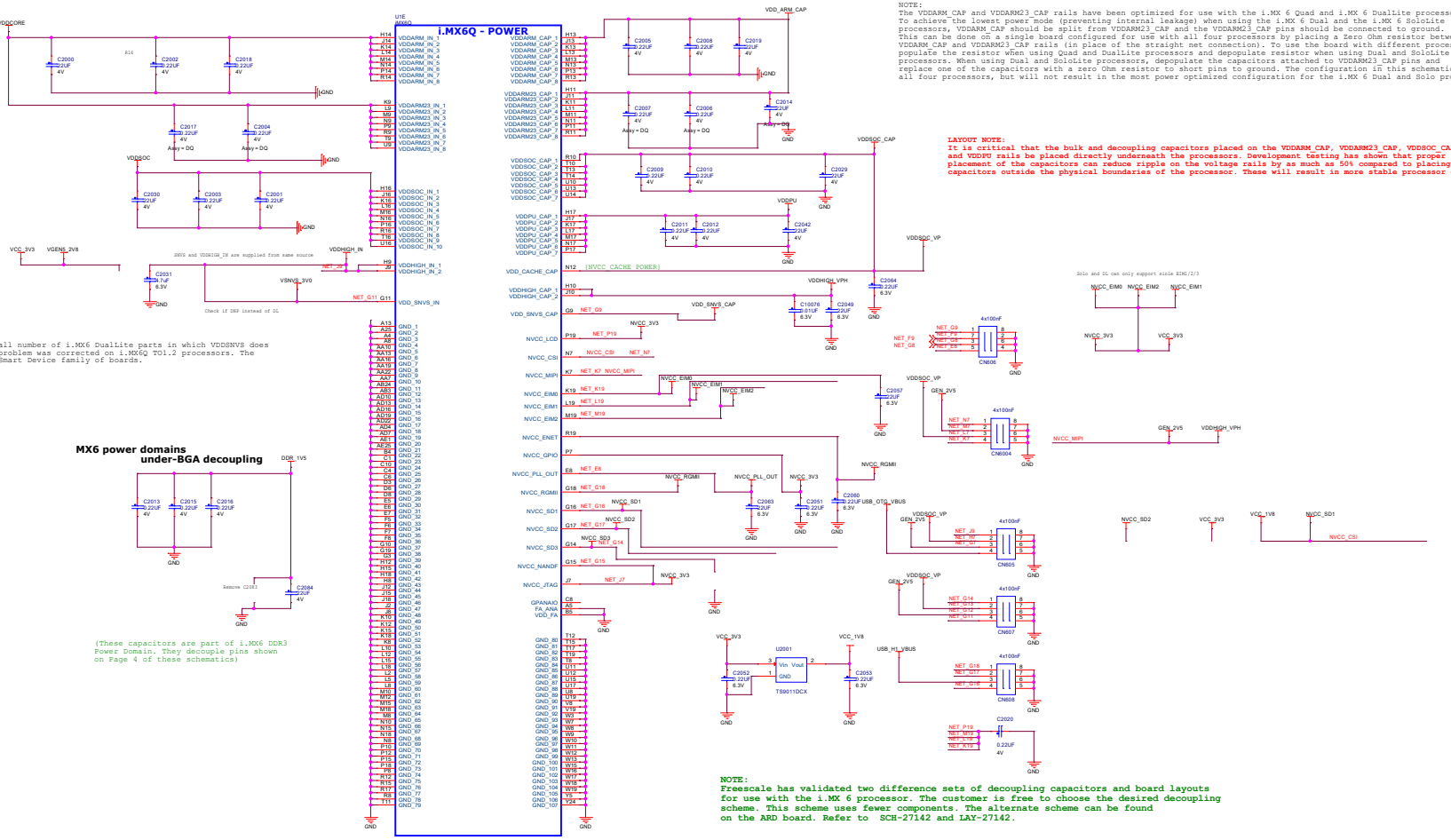
ICAP Classification: FCP: FIUO: PUBI: X

Designer: Mark Middleton	Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM
Drawn by: Mark Middleton	Page Title: TITLE PAGE
Approved: <Approver>	Size: D; Document Number: SOURCE:SCH-27362 PDF:SPF-27362; Rev: C2
	Date: Monday, May 18, 2015; Sheet 1 of 10



NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 Duallite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q TO1.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the ARD board. Refer to SCH-27142 and LAY-27142.

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ICAP Classification:	FCP: FUO: PUB: X
Drawing Title:	MCIMX6Q-SMART DEVICE PLATFORM
Page Title:	CPU POWER
Size: D	Document Number: SOURCE:SCH-27362 PDF:SPF-27362 Rev: C2
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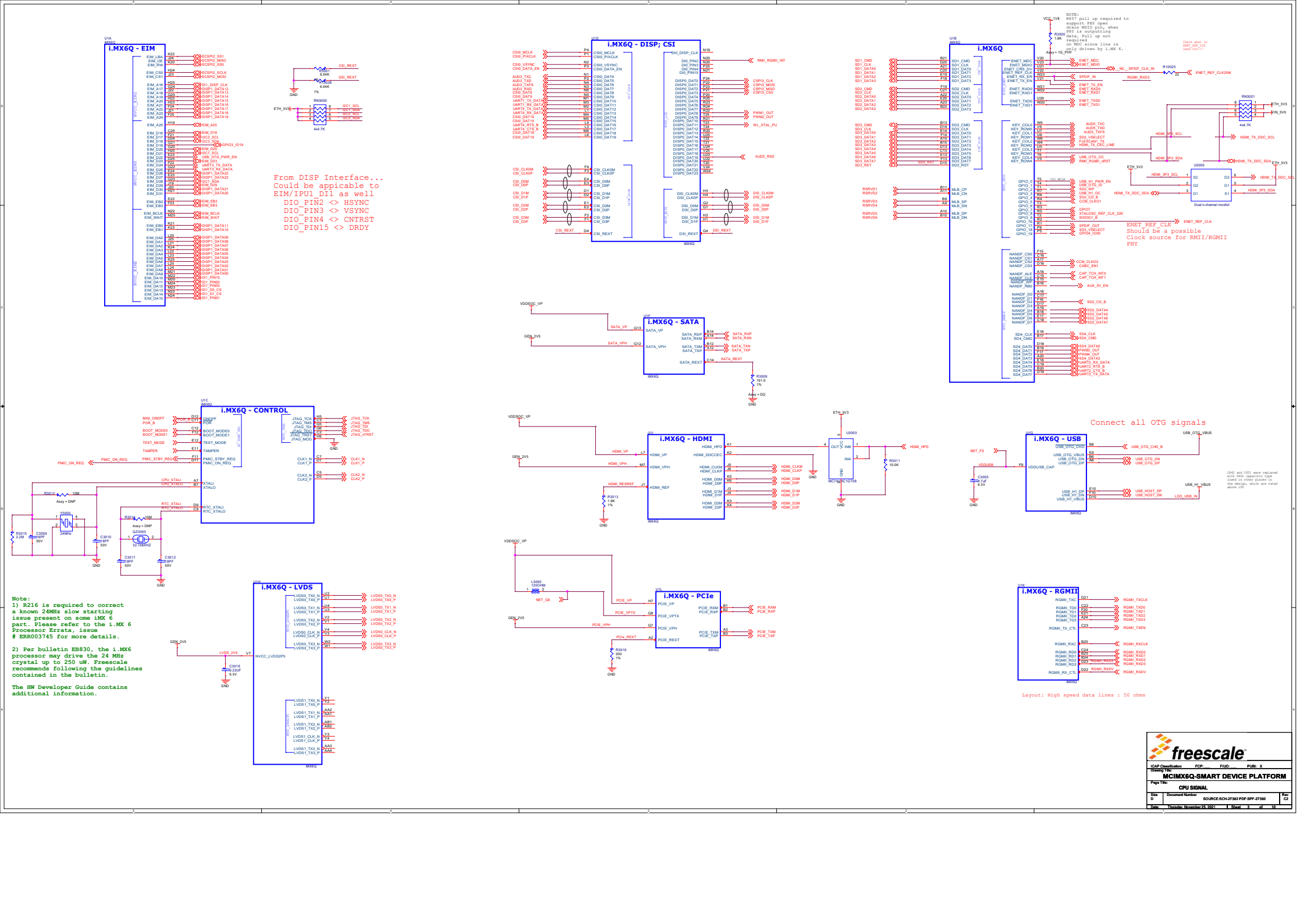
i.MX6Q - EIM
i.MX6Q - DISP; CSI
i.MX6Q
i.MX6Q - SATA
i.MX6Q - CONTROL
i.MX6Q - HDMI
i.MX6Q - USB
i.MX6Q - LVDS
i.MX6Q - PCIe
i.MX6Q - RGMII
From DISP Interface...
Could be appicable to
EIM/IPU1_DI1 as well
DIO_PIN2 <> HSYNC
DIO_PIN3 <> VSYNC
DIO_PIN4 <> CNTRST
DIO_PIN15 <> DRDY
NOTE:
R657 pull up required to
support PHY open
drain MDIO pin, when
PHY is outputting
data. Pull up not
required
on MDC since line is
only driven by i.MX 6.
Assy = 1G_PHY
ENET_REF_CLK
Should be a possible
Clock source for RMII/RGMII
PHY
Connect all OTG signals
Note:
1) R216 is required to correct
a known 24MHz slow starting
issue present on some iMX 6
part. Please refer to the i.MX 6
Processor Errata, issue
ERR003745 for more details.
2) Per bulletin EB830, the i.MX6
processor may drive the 24 MHz
crystal up to 250 uW. Freescale
recommends following the guidelines
contained in the bulletin.
The HW Developer Guide contains
additional information.
Layout: High speed data lines : 50 ohms
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ICAP Classification: FCP: FUD: PUB: X
Drawing Title:
MCIMX6Q-SMART DEVICE PLATFORM
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CPU SIGNAL
Size D
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Clock terminators: Place at end of route at each DDR pair

DRAM_SDCLK0 — R4000 200 1% — DRAM_SDCLK0_B
DRAM_SDCLK1 — R4001 200 1% — DRAM_SDCLK1_B
Assy = DDR64

U1J
iMX6Q

i.MX6Q - DDR

DRAM_D[63:0]
DRAM_A[15:0]

U4001 — 2G_DDR3_SDRAM_128MX16 — K4B4G1646B
U4002 — 2G_DDR3_SDRAM_128MX16 — K4B4G1646B
U4003 — 2G_DDR3_SDRAM_128MX16 — K4B4G1646B
U4004 — 2G_DDR3_SDRAM_128MX16 — K4B4G1646B

DDR_1V5
DDR_VREF
GND

Clock access points

R4004 10.0K 1%
R4005 10.0K 1%
R4002 200 1%
R4003 200 1%
R4006 240 1%
R4007 240 1%
R4008 240 1%
R4009 240 1%
R4010 240 1%

C4000 0.22UF 6.3V
C4001 0.1UF 16V
C4002 0.22UF 6.3V
C4004 0.1UF 16V
C4005 0.22UF 6.3V
C4007 0.22UF 6.3V
C10021 0.22UF 4V
C10022 0.22UF 4V
C10024 0.22UF 4V
C10026 0.22UF 4V
C10031 0.22UF 4V
C10032 0.22UF 4V
C10033 0.22UF 4V
C10037 0.22UF 4V
C10038 0.22UF 4V
C10039 0.22UF 4V
C10040 0.22UF 4V
C10041 0.22UF 4V
C10042 0.22UF 4V
C10043 0.22UF 4V
C10044 0.22UF 4V
C10046 0.22UF 4V
C10047 0.22UF 4V
C10050 0.22UF 4V

Assy = DDR64

NOTE 1:

Using bit swapping for DATA bus to allow easy pcb routing.

When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.

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Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: DDR3 MEMORY

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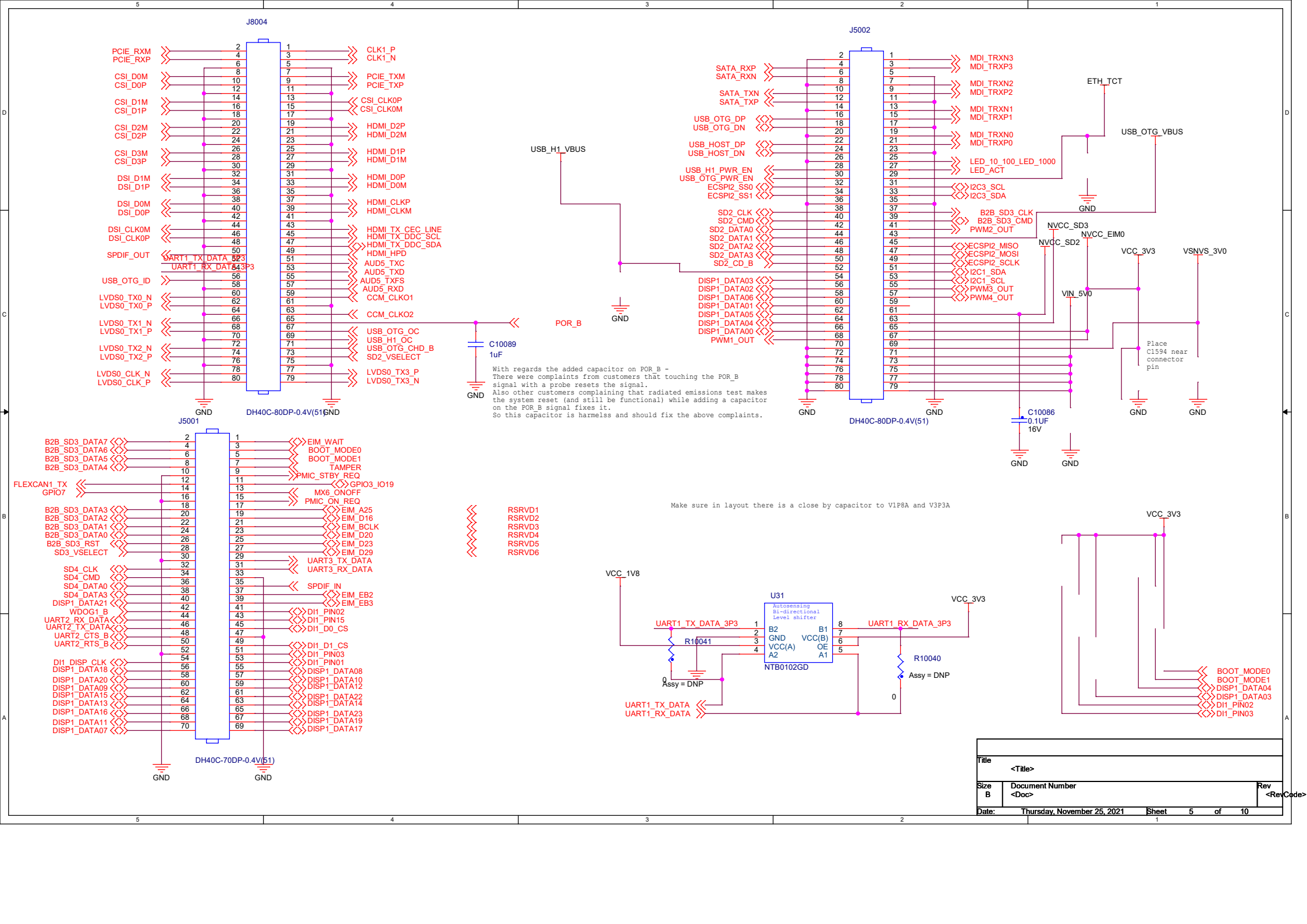

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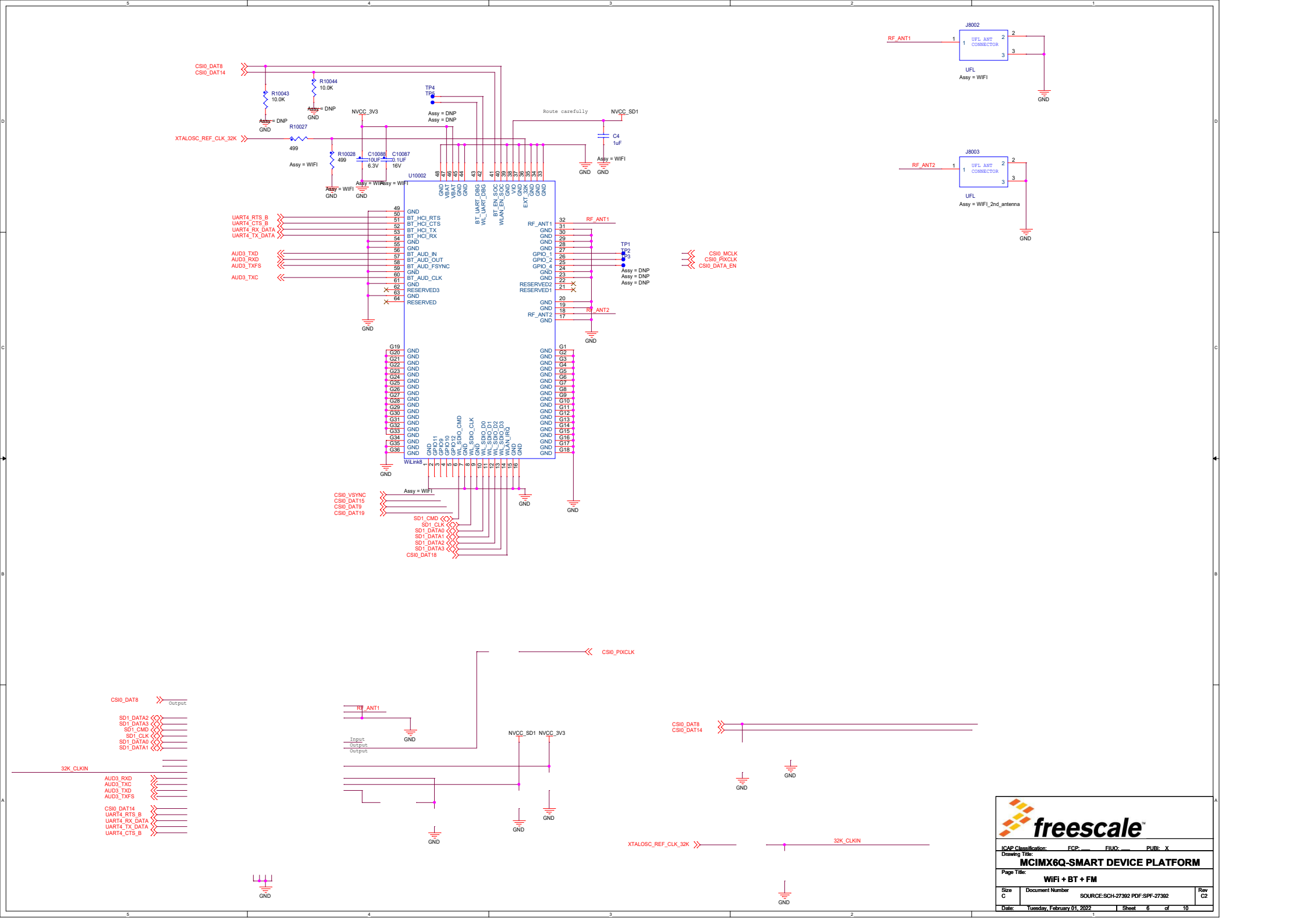
J8002
RF_ANT1
UFL ANT CONNECTOR
UFL
Assy = WIFI
GND
J8003
RF_ANT2
UFL ANT CONNECTOR
UFL
Assy = WIFI_2nd_antenna
GND
CSI0_DAT8
CSI0_DAT14
R10043 10.0K
R10044 10.0K
Assy = DNP
GND
TP4
TP5
NVCC_3V3
Route carefully
NVCC_SD1
C4 1uF
XTALOSC_REF_CLK_32K
R10027 499
R10028 499
C10088 10UF 6.3V
C10087 0.1UF 16V
Assy = WIFI
U10002
WiLink8
UART4_RTS_B
UART4_CTS_B
UART4_RX_DATA
UART4_TX_DATA
AUD3_TXD
AUD3_RXD
AUD3_TXFS
AUD3_TXC
BT_HCI_RTS
BT_HCI_CTS
BT_HCI_TX
BT_HCI_RX
BT_AUD_IN
BT_AUD_OUT
BT_AUD_FSYNC
BT_AUD_CLK
RESERVED3
RESERVED
RF_ANT1
RF_ANT2
GPIO_1
GPIO_2
GPIO_4
RESERVED2
RESERVED1
TP1
TP2
TP3
CSI0_MCLK
CSI0_PIXCLK
CSI0_DATA_EN
CSI0_VSYNC
CSI0_DAT15
CSI0_DAT9
CSI0_DAT19
SD1_CMD
SD1_CLK
SD1_DATA0
SD1_DATA1
SD1_DATA2
SD1_DATA3
CSI0_DAT18
32K_CLKIN
Output
Input
Output
Output
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ICAP Classification: FCP: ___ FIUO: ___ PUBI: X
Drawing Title:
MCIMX6Q-SMART DEVICE PLATFORM
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WiFi + BT + FM
Size C
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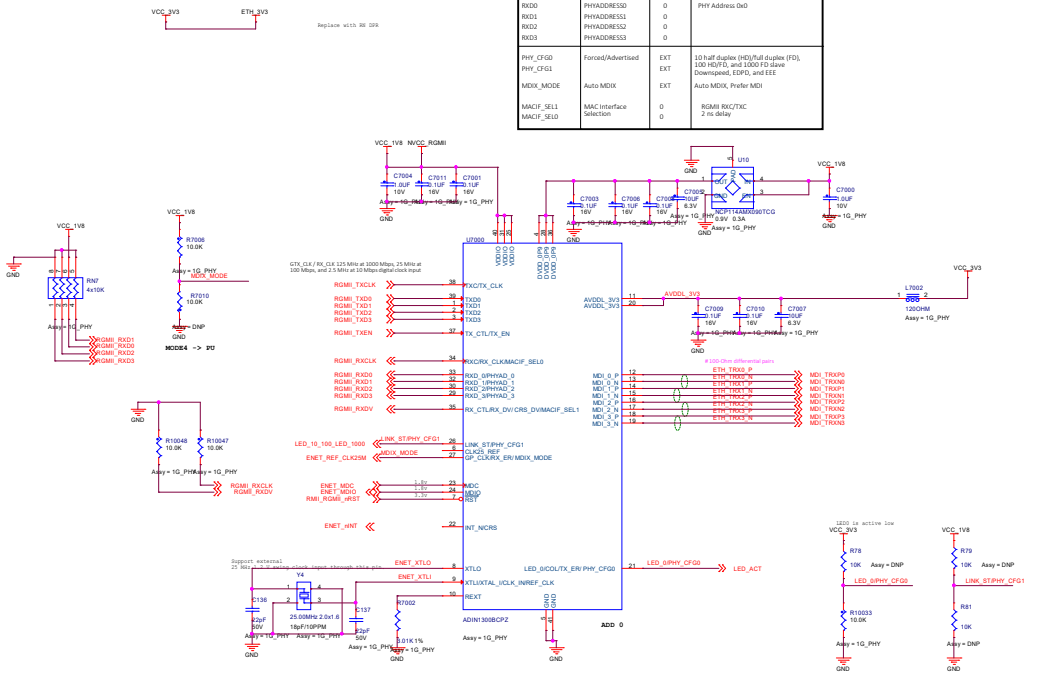
PHY PIN	PHY CFG	Default	Default Configuration
RXD0	PHYADDRESS0	0	PHY Address 0x0
RXD1	PHYADDRESS1	0	
RXD2	PHYADDRESS2	0	
RXD3	PHYADDRESS3	0	
PHY_CFG0	Forced/Advertised	EXT	10 half duplex (HD)/full duplex (FD), 100 HD/FD, and 1000 FD slave Downspeed, EDPD, and EEE
PHY_CFG1		EXT	
MDIX_MODE	Auto MDIX	EXT	Auto MDIX, Prefer MDI
MACIF_SEL1	MAC Interface Selection	0	RGMII RXC/TXC 2 ns delay
MACIF_SEL0		0	



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Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: ETHERNET

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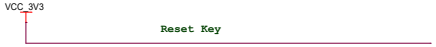
JTAG

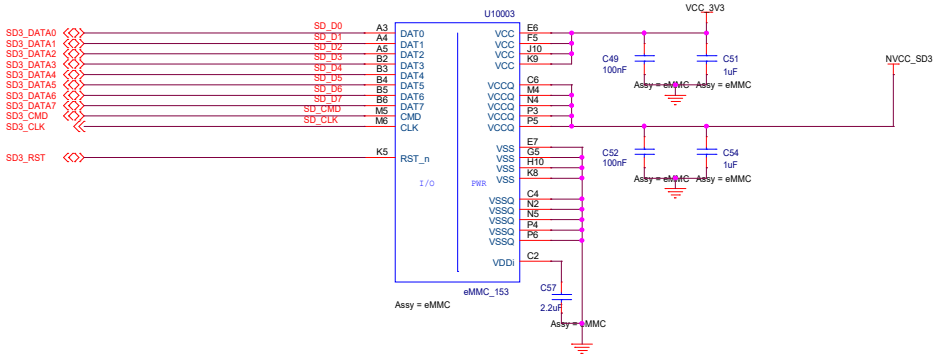
JTAG



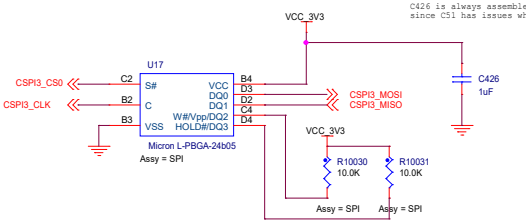
This is mandatory pull down; or can be directly connected to GND (check spec); this can also be combined with other resistors

Not placed short.
Can be used to force NVCC_SD3 (eMMC interface) to VCC_3V3

C51 is not assembled anymore since it has mechanical issues when being assembled with the board to board header on the carrier side. Instead C426 is always assembled



C426 is always assembled. It covers the SPI and eMMC 3.3v since C51 has issues when being assembled.



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Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: JTAG, DEBUG

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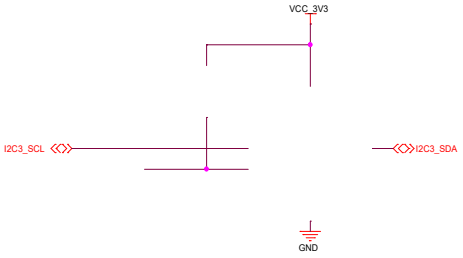

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Drawing Title:
MCIMX6Q-SMART DEVICE PLATFORM

Page Title:
BOOT SELECT

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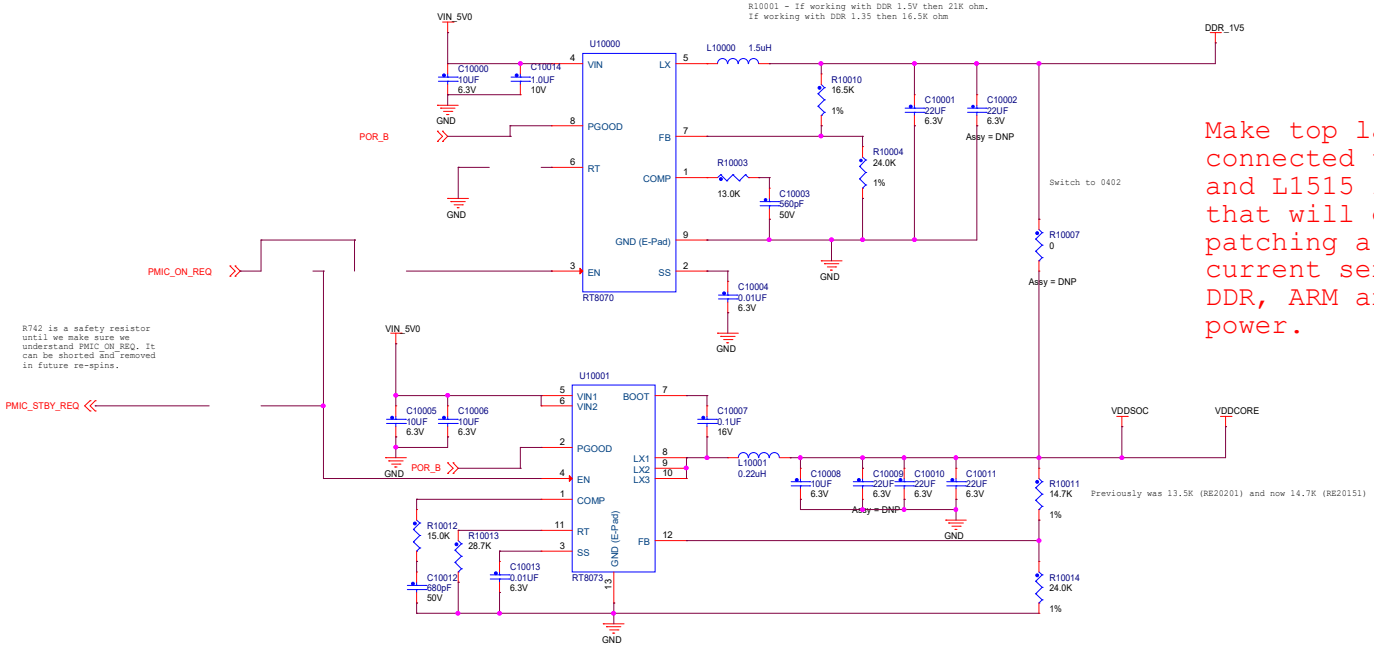

Make top layer planes connected to L1514 and L1515 in a way that will enable patching a board for current sensing or DDR, ARM and SOC power.

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Drawing Title: MCIMX6Q-SMART DEVICE PLATFORM

Page Title: eMMC, SPI NOR FLASH

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